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All-optical digital logic and neuromorphic computing based on multi-wavelength auxiliary and competition in a single microring resonator

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Photonic hardware implementation of spiking neural networks, regarded as a viable potential paradigm for ultra-high speed and energy efficiency computing, leverages spatiotemporal spike encoding and event-driven dynamics to simulate brain-like parallel information processing. Silicon-based microring resonators (MRRs) offer a power efficiency and ultrahigh flexibility scheme to mimic biological neuron, however, their substantial potential for integrated neuromorphic systems remains limited by insufficient exploration of MRR-based spiking digital and analog computation. Here, an all-optical neural dynamics framework, encompassing both excitatory and inhibitory behaviors based on multi-wavelength auxiliary and competition mechanism in an MRR, is proposed numerically. Leveraging multi-wavelength resonance characteristics and wavelength division multiplexing (WDM) technology, a single MRR implements the five fundamental optical digital logic gates: AND, OR, NOT, XNOR and XOR. Besides, the cascading capabilities of MRR-based spiking neurons are demonstrated through multi-level digital logic gates including NAND, NOR, 4-input AND, 8-input AND, and a full adder, emphasizing their promise for large-scale digital logic networks. Furthermore, an exemplary binary convolution has been achieved by utilizing the proposed MRR-based digital logic operation, illustrating the potential of all-optical binary convolution to compute image gradient magnitudes for edge detection. Such passive photonic neurons and networks promise access to the high transmission speed and low power consumption inherent to optical systems, thus enabling direct hardware-algorithm co-computation and accelerating artificial intelligence.

Keywords: photonic neuron; spiking neural network; microring resonator; optical computing; artificial intelligence

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Introduction

Artificial intelligence (AI) technologies that perform computations on von Neumann architectures have revolutionized various aspects of human society and scientific domain like financial transactions[1], biomedical research[2,3], weather forecasting[4], image recognition[5,6], chaos synchronization[7,8], etc., yet they still face persistent challenges in processing speed and power efficiency because of the inherent limitations arising from the separation between the processing unit and memory in traditional computing systems. Inspired by the hierarchical structure and event-driven asynchronous information processing of the human brain, spiking neural networks (SNNs) have been proposed as a promising alternative to

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address the fundamental dilemmas of traditional computing architectures. Due to the rich spatiotemporal dynamics, sparse spike transmission, bio-realistic properties, and event-driven manner, SNNs exhibit an ultra-low power biological foundation and notable interpretability, thus garnering extensive attention in scientific communities[9–14]. Recently, substantial advances have been made in electronic neuromorphic systems, exemplified by platforms such as SpiNNaker[15], Neurogrid[16], TrueNorth[17], Loihi[18], and Tianjic[19]. However, conventional electronic neuromorphic systems are constrained by factors such as low bandwidth efficiency, limited parallelism, and high processing delays, which restrict their computational speed and power efficiency in ultrafast artificial intelligence fields. As a promising alternative, photonic counterparts offer great opportunities for next-generation neuromorphic architectures due to their advantages such as exceptionally high bandwidth, minimal energy consumption, massive parallelism, and negligible electromagnetic interference, enabling functions such as matrix multiplication, optical logic operations, and the emulation of neuromorphic functions. These unique capabilities contribute to overcoming the limitations imposed by the electronic bottleneck and significantly enhance computing performance, making the implementation of SNNs through photonic hardware a promising avenue for advancing AI technologies.

In pursuit of this vision, various photonic neuromorphic devices have been proposed and developed to physically realize the computational primitives required by SNNs. As a pivotal element in photonic SNNs, both the theoretical models and hardware implementation of neurons—often regarded as ultra-fast nonlinear computational units—have garnered significant attention. As illustrations, some semiconductor lasers such as vertical-cavity surface-emitting laser with an embedded saturable absorber (VCSEL-SA) exhibit intrinsic nonlinear spiking dynamics analogous to those observed in biological neurons, and play pivotal roles in photonic neuromorphic computing. Subsequently, extensive research has been devoted to leveraging these active device-based spiking neurons for constructing SNNs architectures and performing neuromorphic information processing tasks[20–29]. However, the requirement for electrical biasing and external driver circuit in active device-based spiking neuron poses challenges in power efficiency, system compactness, and large-scale integration. These limitations have motivated growing interest in passive device-based neuron implementations, which exhibit strong compatibility with mainstream silicon platforms and offer substantial potential for achieving large-scale integration and energy-efficient photonic SNNs. For example, passive phase-change materials (PCMs) play a critical role in neuromorphic computing. Their reversible amorphous-crystalline transitions enable the emulation of spiking neurons and synapses in photonic SNNs, thereby supporting scalable circuit architectures and enabling pattern recognition[30]. MRRs, another representative class of passive devices, feature a compact footprint, compatibility with WDM, and high tunability, making them widely adopted in photonic neuromorphic systems[31,32]. Although an all-optical spiking neuron has been theoretically investigated and experimentally demonstrated by leveraging the interplay between fast free-carrier dynamics and slow thermal effects in passive silicon add-drop MRRs (ADMRRs)[33–39], their cascading capability and inhibitory dynamics for realizing complex computational tasks remain insufficiently explored. Simultaneously, despite the demonstrated potential of MRR-based spiking neurons, current research has been confined to single-wavelength excitation schemes. In contrast, multi-wavelength injection approaches—which promise to unlock higher-dimensional computational capabilities and richer neurodynamic behaviors—have received little attention. This critical gap calls for comprehensive investigations to fully harness the potential of multi-wavelength-driven photonic spiking neurons.

Here, to the best of our knowledge, we present the first systematic demonstration of nonlinear-induced neural dynamics in a passive ADMRR by harnessing multi-wavelength auxiliary and competition mechanisms. To transcend the limitations of prior single-wavelength analyses and to provide a unified theoretical framework for understanding the multi-resonant behavior of ADMRR-based spiking neurons, we further develop a universal coupled mode theory (CMT) framework for all passive side-coupled microresonators under multi-resonant light injection conditions. Building upon this theoretical foundation, a variety of neural dynamics—including self-pulsation, excitatory and inhibitory responses, as well as cascading capability—are demonstrated in the exemplary ADMRR-based spiking neuron under multi-wavelength injection, enabled by the interplay of auxiliary and competitive optical inputs. These controllable neurodynamic behaviors provide a functional foundation for implementing digital logic primitives in the optical domain.

By leveraging our proposed spike encoding rules, the ADMRRs-based spiking neurons are applied to achieve fundamental neuromorphic digital logic operations, including AND, OR, NOT, XOR, and XNOR. Subsequently, the cascading functionality of ADMRR-based spiking neurons facilitates the realization of a multi-level neuromorphic digital logic operation. The implementation of NAND gate, NOR gate, 4-input AND gate, 8-input AND gate, and a full adder is validated, highlighting the potential of the proposed scheme for scaling complex digital network computations. Furthermore, all-optical neuromorphic binary convolution with ADMRR-based spiking neurons for image gradient magnitudes is demonstrated, showcasing that our proposed ADMRRs-based neuron has the capability of co-computing hardware algorithms for accomplishing AI tasks. Combined with the WDM technology, the multi-wavelength neurons present a promising avenue toward hardware-software co-design and optimization of multilayer passive SNNs, opening new opportunities for digital computation and brain-inspired neuromorphic systems.

Methods

Theoretical model

The proposed all-optical spiking neuron based on an ADMRR by harnessing multiple resonant wavelengths auxiliary and competition mechanisms is presented schematically in Fig. 1. The nonlinear computational functions of the MRRs-based spiking neuron, such as self-pulsation, excitability, and refractory periods, have been theoretically investigated and experimentally demonstrated across diverse integrated Silicon-On-Insulator (SOI) MRRs[33–40]. These nonlinear phenomena are induced by the combined impacts of two-photon absorption (TPA), free carrier absorption (FCA), free carrier dispersion (FCD), and thermal nonlinearity. Notably, previous investigations into MRR-based spiking neurons have predominantly centered on single-wavelength inputs, largely neglecting the nonlinear dynamics elicited by multiple resonant wavelength interactions. However, the incorporation of multiple resonant wavelength optical inputs markedly improves the nonlinear response flexibility of MRRs, enhances parallel computational capacity, and optimizes device efficiency, underscoring their potential for advancing passive spiking neuron applications. Here, building upon the reported CMT for passive side-coupled microresonators[34–37,40–48], we first propose, to best our knowledge, a universal CMT model for all passive microresonators-based spiking neuron with multiple resonant wavelengths, and the nonlinear dynamics of the wavelength-multiplexed microresonator can be described as follows:

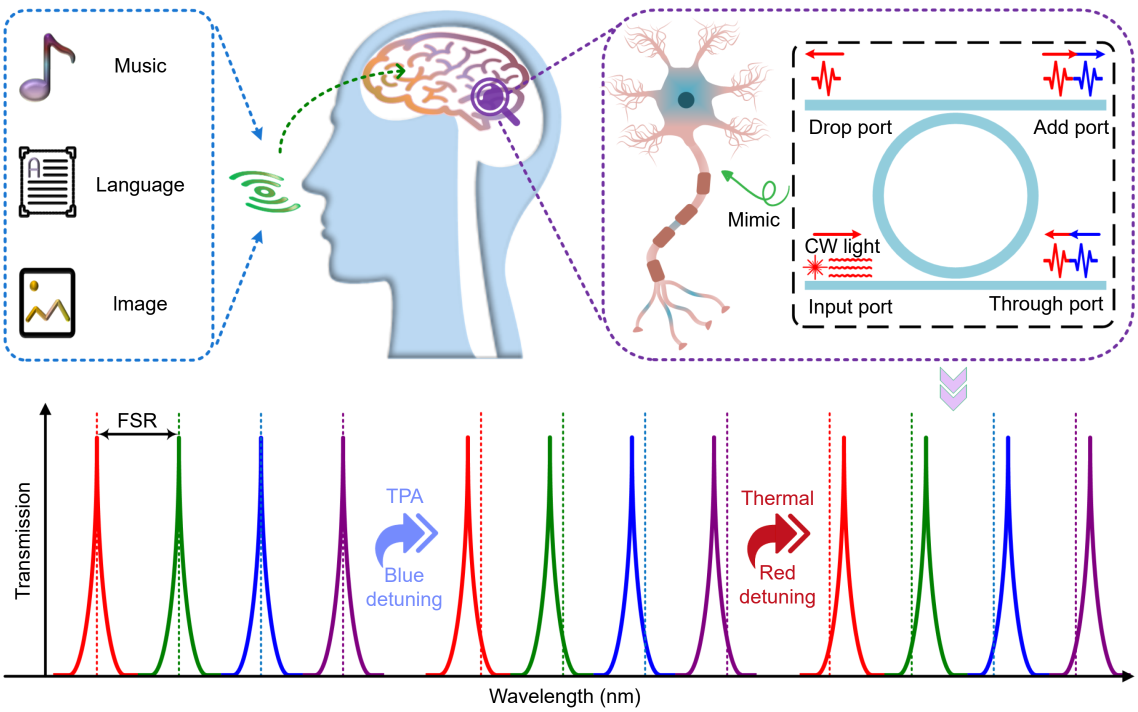

Fig. 1 | Conceptual diagram of a passive wavelength-multiplexed spiking neuron leveraging ADMRRs.

$$\frac{\mathrm{d}a_{\lambda_l,+}}{\mathrm{d}t} = [\mathrm{j}(\omega_{\lambda_l,R} + \delta\omega_{\lambda_l,+} - \omega_{\lambda_l,+}) - \frac{\gamma_{\lambda_l,+,\text{total}}}{2}]a_{\lambda_l,+} + \kappa_{\lambda_l,+}S_{\lambda_l,+}, \quad \text{where, } l = 1, 2, 3, 4, \ldots\ldots \tag{1}$$

$$\frac{\mathrm{d}a_{\lambda_i,-}}{\mathrm{d}t} = [\mathrm{j}(\omega_{\lambda_i,R} + \delta\omega_{\lambda_i,-} - \omega_{\lambda_i,-}) - \frac{\gamma_{\lambda_i,-,\text{total}}}{2}]a_{\lambda_i,-} + \kappa_{\lambda_i,-}S_{\lambda_i,-}, \quad \text{where, } i = 1, 2, 3, 4, \ldots\ldots \tag{2}$$

$$\frac{\mathrm{d}N}{\mathrm{d}t} = -\frac{N}{\tau_{\text{fc}}} + \frac{\Gamma_{\text{FCA}}\beta_{\text{Si}}c^2}{2\omega\hbar V_{\text{FCA}}^2 n_g^2}\left(\sum_l |a_{\lambda_l,+}|^2 + \sum_i |a_{\lambda_i,-}|^2\right)^2, \tag{3}$$

$$\frac{\mathrm{d}\Delta T}{\mathrm{d}t} = -\frac{\Delta T}{\tau_{\text{th}}} + \frac{\Gamma_{\text{th}}}{\rho_{\text{Si}}C_{p,\text{Si}}V_{th}}(\gamma_{\pm,\text{lin}} + \gamma_{\pm,\text{FCA}} + \gamma_{\pm,\text{TPA}})\left(\sum_l |a_{\lambda_l,+}|^2 + \sum_i |a_{\lambda_i,-}|^2\right), \tag{4}$$

$$S_{\text{Drop},\lambda_l} = \mathrm{e}^{\mathrm{j}\beta d}(-\kappa_{\text{Drop}}^* \cdot a_{\lambda_l,+}), \tag{5}$$

$$S_{\text{Add},\lambda_i} = \mathrm{e}^{\mathrm{j}\beta d}(+\kappa_{\text{Add}}^* \cdot a_{\lambda_i,-}), \tag{6}$$

within these equations, the symbols "+" and "–" signify the forward and backward directions correspondingly, and the λ_l (λ_i) represents the resonant wavelengths forward (backward) coupled to the ADMRR. Here, a_λ denotes the complex amplitude of the propagation mode corresponding to the light wavelength λ, and N represents the density of free carriers within the ADMRR. Additionally, S_+ (S_-) is the complex amplitudes of pump (auxiliary) light, while, S_{Drop} (S_{Add}) indicates the complex amplitude of the output light at the 'Drop' ('Add') port. Several other key parameters are involved, including the cold resonance frequency ω_{R}, the nonlinear frequency shift $\delta\omega$, the frequency of input light in the waveguide ω, the mode-averaged temperature difference with the environment ΔT, the relaxation time for temperature τ_{th}, the effective free-carrier decay rate τ_{fc}, the density of silicon ρ_{Si}, the thermal capacity of silicon $C_{p,\text{Si}}$, the effective mode volume V, the confinement coefficient Γ, the propagation constant in the output waveguide β, the finite distance between the reference planes d, the coupling coefficient κ, the constant governing two-photon absorption β_{Si}, the velocity of light c, the group index n_g, the total loss for the cavity mode $\gamma_{\pm,\text{total}}$, the $\gamma_{\pm,\text{line}}$ denotes the linear absorption loss, the $\gamma_{\pm,\text{FCA}}$ and $\gamma_{\pm,\text{TPA}}$ are the loss due to the FCA effect and the TPA effect, respectively.

As shown in Eqs. (3) and (4), optical signals at all resonant wavelengths couple into the ADMRR, where free carriers N are first generated via TPA effect and subsequently depleted through FCA effect. In parallel, optical signals from multiple wavelength channels are absorbed during propagation within the ADMRR and converted into thermal energy. Consequently, optical signals at all wavelengths interact through both auxiliary and competitive inputs, collectively influencing the neurodynamic behavior of the ADMRR. It is worth noting that, in practice, wavelength-dependent material dispersion and fabrication tolerances can introduce asymmetric variations in the resonant cavity parameters, resulting in slight deviations in the excitability thresholds across different wavelengths. However, such deviations exert no fundamental impact on the operational principles underpinning the realization of subsequent digital logic gates. Therefore, the parameters of a single ADMRR are assumed to remain approximately invariant across wavelengths to facilitate analysis. Furthermore, the simulation parameters utilized in this work replicate those documented in earlier studies[34–37,41], with several key parameters summarized in Table 1.

All-optical digital logic operation

Figure 2 is the schematic framework for fundamental all-optical digital logic operations, encompassing AND, OR, NOT, XNOR, and XOR gates, implemented via a single ADMRR driven by dual-resonant wavelength inputs. In the proposed all-optical digital logic gates, a continuous-wave (CW) light at resonant wavelength λ_1, with power below the nonlinear-induced self-pulsation threshold, is inputted into the 'Input' port of the ADMRR. Perturbation pulses at wavelengths λ_1 and λ_2, encoded with distinct strategies, are injected from the 'Through' port, enabling the realization of five fundamental digital logic operations. Figure 2(a) presents the implementation of the AND logic. Perturbation pulses encoded at λ_1 and λ_2, with power levels above half but below the excitability threshold, are injected via the 'Through' port. Spiking at the 'Drop' port occurs only when both pulses coincide, indicating a logical output of '1'; otherwise, the output is '0'. In Fig. 2(b), the power of the two encoded rectangular pulses fed into the 'Through' port of the OR gate is set to slightly exceed the excitability threshold, and the rest of the configuration remains unchanged from the AND gate structure. The neural spikes are generated at the 'Drop' port when either or both rectangular pulses are present, indicating a logical output of '1'; otherwise, the

Table 1 | Main parameters of ADMRR and photonic crystal[34–37,41].

Parameters	ADMRR	Photonic crystal
λ_R	1550 nm/1568 nm	1552.45 nm/1571.4 nm
τ_{th}	65 ns	~20 ns
τ_{fc}	5.5 ns	0.5 ns
ρ_{Si}	2.33 g/cm^3	2.33 g/cm^3
$C_{p,\text{ Si}}$	0.7 J/(g·k)	0.7 J/(g·k)
V_{th}	3.81 μm^3	0.48 μm^3
V_{FCA}	2.82 μm^3	0.40 μm^3
Γ_{th}	0.934	0.965
Γ_{TPA}	0.995	0.982
Γ_{FCA}	0.998	0.997
β_{Si}	8.4×10^{-12} m/W	8.4×10^{-12} m/W
n_g	3.476	3.476
σ_{Si}	10^{-21} m^2	10^{-21} m^2
n_2	4.5×10^{-18} m^2/W	4.5×10^{-18} m^2/W
dn_{Si}/dT	0.000186 K^{-1}	0.000186 K^{-1}
γ_{line}	3.9024×10^9	0.86×10^9

output is '0'. In contrast, the NOT gate exploits the inhibitory dynamics of the ADMRR. Here, the 'Through' port inputs two perturbations that exceed the excitability threshold power, with a temporal offset between them. For simplicity, we assume that the perturbation pulse at wavelength λ_1 precedes the perturbation pulse at wavelength λ_2. When the λ_1 pulse is present, the input of the NOT gate is regarded as '1', and the 'Add' port does not produce a spike at wavelength λ_2, resulting in a logic output of '0'. Conversely, when the λ_1 pulse is absent, the NOT input is treated as '0', and the 'Add' port emits a spike at λ_2, leading to a logic output of '1'.

Furthermore, a hardware architecture enabling efficient XOR and XNOR operations is proposed by leveraging our temporal encoding strategy and the neural dynamics of the ADMRR-based spiking neuron. The schematics of the XNOR and XOR operators based on a passive ADMRR are depicted in Fig. 2(d) and 2(e), respectively. Initially, binary digital signals ('0' and '1') are transformed into temporally encoded optical rectangular pulses at wavelengths λ_1 and λ_2. A temporal encoding window, T_w, is defined and divided into two equal

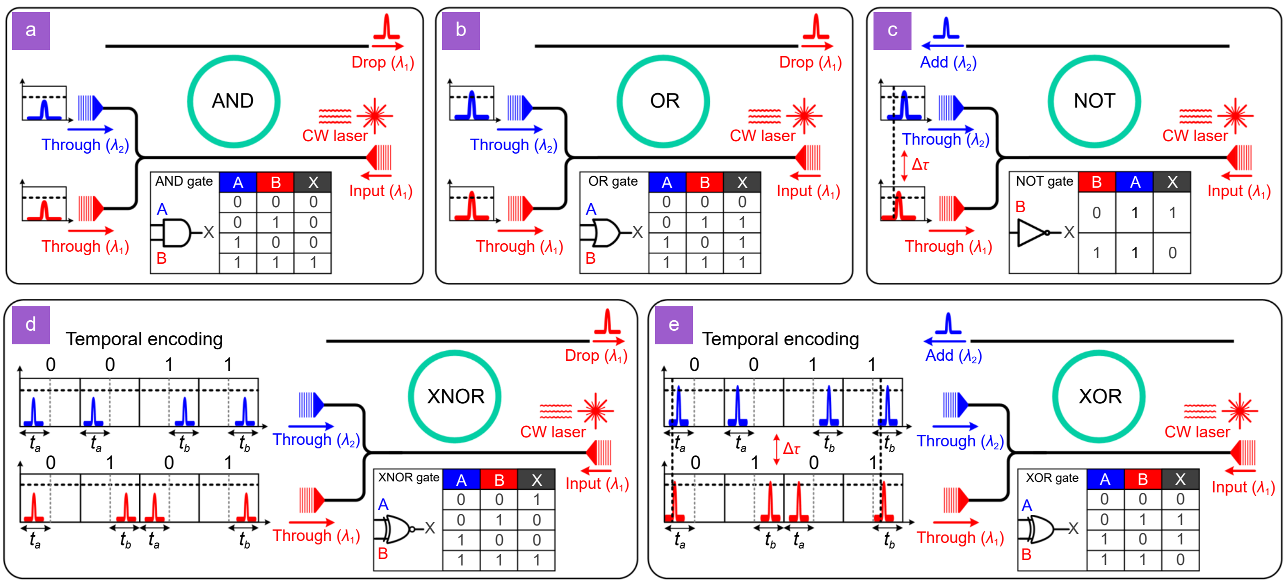

Fig. 2 | Schematic of all-optical digital logic gates realized using a single ADMRR. (**a**) AND gate, (**b**) OR gate, (**c**) NOT gate, (**d**) XNOR gate, and (**e**) XOR gate.

sub-intervals centered at, t_a and t_b, where $t_a < t_b$. Subsequently, the center timings of the optical rectangular pulses at λ_1 and λ_2, corresponding to '0' and '1', are aligned with t_a and t_b, respectively. These encoded pulse sequences are injected into the 'Through' ports of the ADMRR. For the XNOR operation, the encoded optical perturbation pulses are set to power levels below the spiking threshold of the ADMRR-based neuron but exceed half of that threshold. When optical perturbation pulses at both λ_1 and λ_2 are present simultaneously at either t_a or t_b, a spike is generated at the 'Drop' port within T_w period, indicating a logical operation output of '1'; otherwise, the logical operation results in '0'. In configuring the XOR gate, the power of the encoded optical perturbation pulse at λ_1 injected into the 'Through' port is set to surpass the threshold power required for spiking responses, while the encoded optical perturbation pulse at λ_2 injected into the 'Through' port not only exceeds the threshold power but also experiences a temporal t_{delay} delay, falling within the inhibitory window afterward. When both rectangular pulses at wavelengths λ_1 and λ_2 coincide simultaneously at t_a or t_b, the absence of spike responses within the T_w duration at the 'Add' port indicates a logical operation outcome of '0'; otherwise, the operation results in '1'.

Cascaded all-optical digital logic operation

The multi-level cascading of digital logic operations is a pivotal strategy for enhancing computational capacity and implementing complex logic functions within digital logic networks, which indicates the necessity of exploring the cascading behavior in the proposed ADMRRs-based digital logic gates. Figure 3 illustrates three cascaded configurations of all-optical digital logic gates, including a 4-input AND gate, a NAND gate, and a NOR gate. In the 4-input AND gate shown in Fig. 3(a), two first-layer AND gates are cascaded into a second-layer AND gate via their 'Drop' ports. To enable proper operation, distinct wavelengths are assigned to the first-layer gates, and their output spikes are calibrated below the excitation threshold of the second-layer gate but above half of it. This ensures that a spike is produced at the second-layer gate only when both first-layer gates are activated. An alternative approach, depicted in the dashed diagram, employs four optical pulses at different wavelengths, each slightly exceeding one-quarter of the threshold power. A spike output is observed only when all pulses align, confirming a logic '1'; otherwise, the output remains '0'.

Furthermore, the investigation of cascading between different logic operations is crucial for the proposed logic gates. Figure 3(b) showcases a NAND logic operation achieved by integrating an AND gate with a NOT gate. The 'Input' ports of AND gate receive two optical pulses, generating a neural spike at its 'Drop' port, which is routed to the NOT gate. At the NOT gate, the neural spike suppresses the optical pulse at the 'Through' port, preventing a neural spike at the 'Add' port and yielding a logic output of '0'. All other input configurations result in an output of '1'. Similarly, Fig. 3(c) presents a NOR logic operation, where an OR gate and a NOT gate are cascaded. When no input optical pulses are applied to the OR gate, the absence of a neural spike at its 'Drop' port leads to a logic output of '1'. Moreover, practical implementations and simulations may leverage optical attenuators and amplifiers to ensure reliable cascading behaviors.

Finally, a representative implementation of a full adder is demonstrated by cascading multiple ADMRR-based spiking neurons. Figure 4(a) presents the structural schematic of the full adder, which is composed of two cascaded half adders and one OR gate by using ADMRR-based spiking neuron. In the proposed full adder architecture, the three input operands—A, B, and Cin—are encoded as spiking inputs and sequentially injected into cascaded ADMRR-based neurons. The first half adder receives A and B as inputs and generates an intermediate sum (S_1) and carry (C_1). The intermediate sum S_1, together with Cin, is then fed into the second half adder, yielding the final sum output (S_2) and a second carry output (C_2). Finally, an ADMRR-based OR gate merges C_1 and C_2 to produce the Cout. Throughout the process, excitatory and inhibitory dynamics are orchestrated via precise multi-wavelength control, enabling accurate and cascadable all-optical logic operations. Moreover, to detail the internal implementation, Fig. 4(b) illustrates the structural schematic of the half adder module in Fig. 4(a), which is composed of an XOR and an AND gate, both realized using ADMRR-based spiking neurons. The XOR gate is particularly critical for sum bit generation, and its implementation is shown in Fig. 4(c). In this configuration, the XOR logic is constructed from two NOT gates, two AND gates, and one OR gate, forming a standard combinational structure. It is noteworthy that spike management in Fig. 4(c) is required at each input port of the cascaded stages to ensure compliance with the encoding rules of the proposed

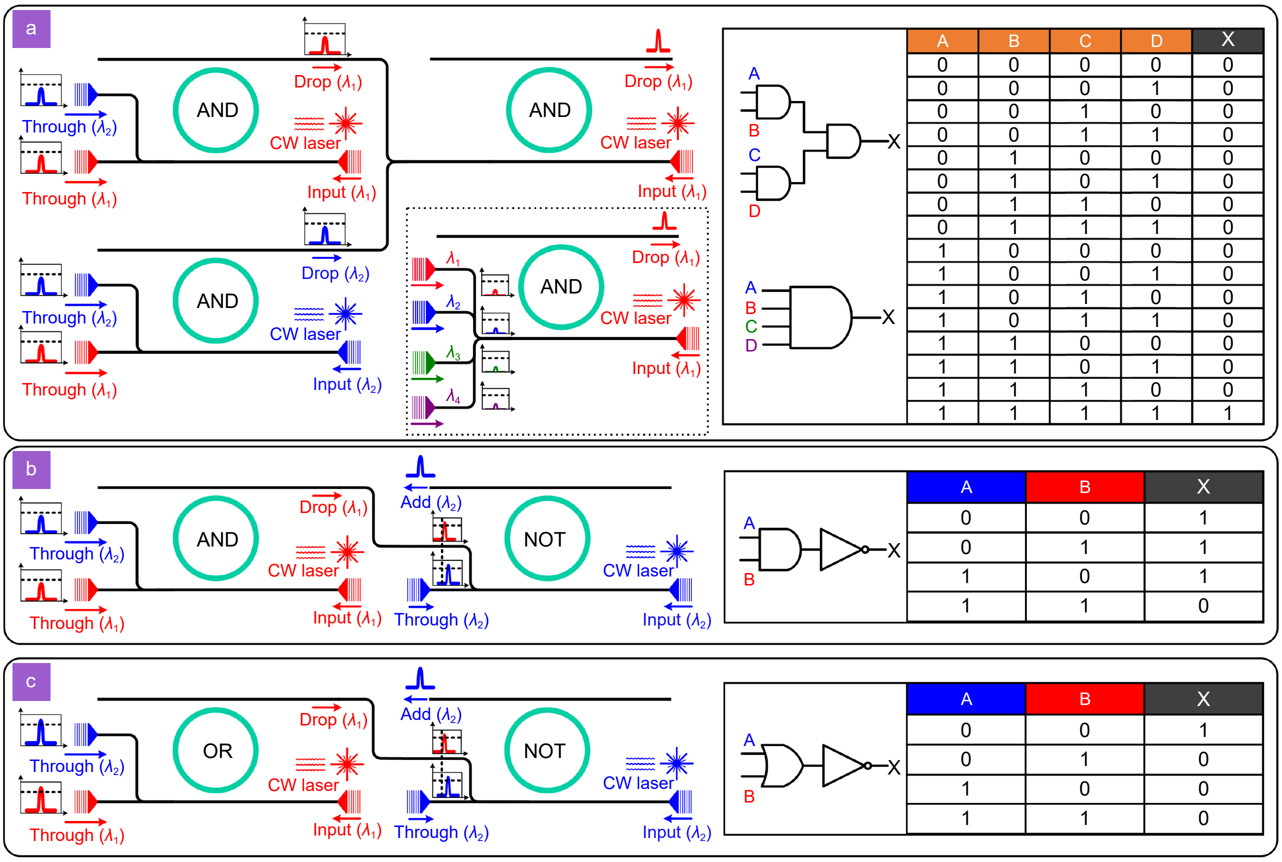

Fig. 3 | Implementation of cascaded all-optical digital logic gates via multi-level configurations. (**a**) 4-input AND gate, (**b**) NAND gate, and (**c**) NOR gate.

logic gates. This spike management involves only simple operations, including linear attenuation, amplification, and temporal delay of the pulses, without altering their temporal shape or functional integrity.

Principle of all-optical binary convolution based on ADMRRs for image gradient magnitudes

In Fig. 5, all-optical binary convolution operations are implemented using the proposed digital logic gates to compute image gradient magnitudes, which are then applied to edge detection. Two distinct schemes—time-division multiplexing (TDM) and WDM—are employed to realize the ADMRR-based convolution functionality. Figure 5(a) shows the implementation of a binary convolution between two 3×3 matrices, one extracted from the source image and the other serving as the convolution kernel, utilizing the TDM approach. Initially, the two matrices are flattened into two one-dimensional vectors to enhance processing efficiency. The nine elements from two vectors are then temporally encoded in each time window t_i (i=1, 2, …, 9), and the encoding rules are consistent with the proposed AND gate in Fig. 2(a). In this binary convolution operation, element-wise multiplication involves only '0' and '1', the output is '1' if and only if both inputs are '1', this operation can be implemented using the AND gate. Consequently, the outputs of the AND operation performed within each of the nine-time windows (t_1 to t_9) are collected as optical spikes. The total number of output spikes across these time slots represents the result of the binary convolution. To further improve processing speed, a WDM-based method is introduced in Fig. 5(b). Compared with Fig. 5(a), the WDM method encodes all nine elements within a single time window, assigning each element a unique wavelength while following the same encoding rules. The elements from the source image and the kernel are mapped to wavelength λ_i and λ_i' (i=1, 2, … , 9), respectively, where λ_i and λ_i' correspond to the two resonant wavelengths of the i-th ADMRR. These encoded signals are simultaneously sent to the ADMRR-based AND gate array, where the element-wise multiplication between image pixels and kernel values is performed all-optically

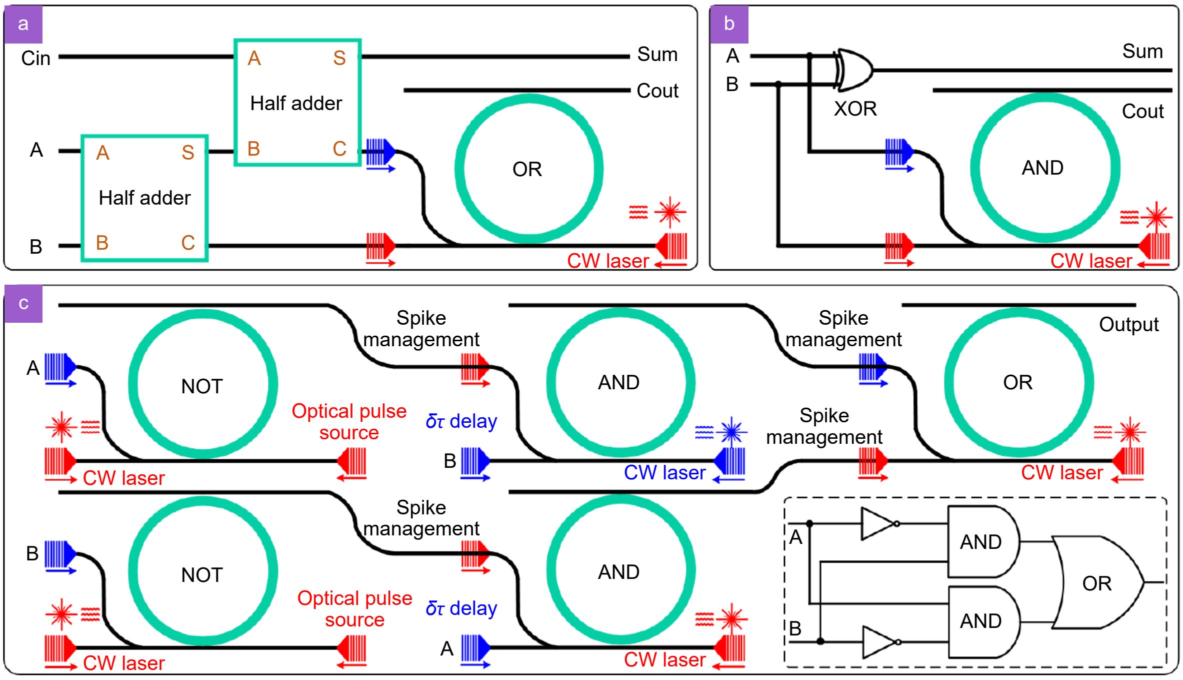

Fig. 4 | Hierarchical construction of arithmetic logic units using ADMRR-based spiking neurons. (**a**) Schematic of a full adder composed of (**b**) a half adder and additional logic, where (b) includes (**c**) an XOR gate as a fundamental component.

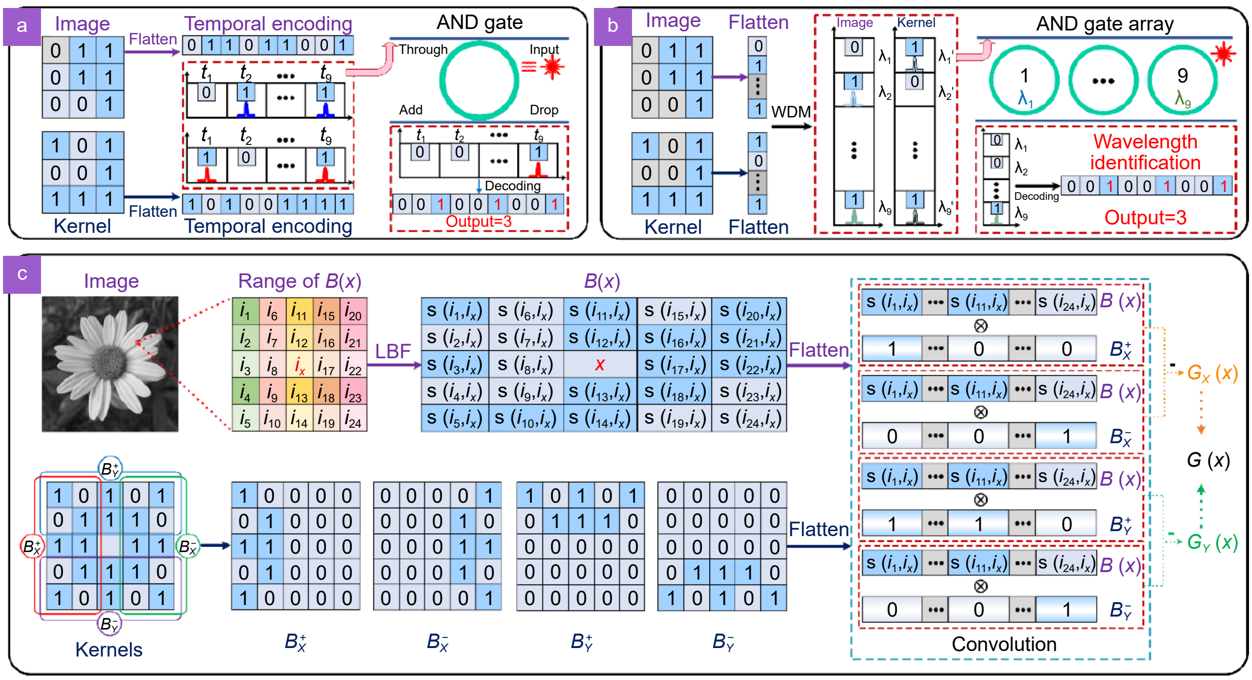

Fig. 5 | Operating principles of the ADMRR-based all-optical binary convolution implemented using (**a**) TDM technology and (**b**) WDM technology. (**c**) Image edge detection process implemented using ADMRR-based spiking neurons in conjunction with a binary gradient estimation algorithm.

in parallel. Ultimately, signals of nine wavelengths are detected at the 'Drop' port, where the number of output spikes is the result of this convolution operation. Then, image gradient magnitudes are calculated and further utilized for optical edge detection, as shown in Fig. 5(c). Specifically, each pixel x corresponds to a 5×5 local binary pattern descriptor $B(x)$ presented in Fig. 5(c). The $B(x)$ is defined in following equations[22,49]:

$$B(x) = \sum_{p=0}^{N-1} s(i_p, i_x) \cdot 2^p, \tag{7}$$

$$s(i_p, i_x) = \begin{cases} 1 & \text{if} \, |i_p - i_x| > T_x \\ 0 & \text{otherwise} \end{cases}, \tag{8}$$

where i_x is the intensity of pixel x, i_p is the intensity of the p-th neighbor of x, $T_x = i_x/4+20$ and $N = 5×5−1$.

Subsequently, $B(x)$ undergoes a binary convolution operation with each of the 5×5 kernels, as highlighted in Fig. 5(c), to extract local features. The gradient magnitude $G(x)$ is then computed using equations as follows[22,49]:

$$G(x) = \sqrt{G_X(x)^2 + G_Y(x)^2}, \tag{9}$$

$$G_X(x) = [B(x) \otimes B_X^+] - [B(x) \otimes B_X^-], \tag{10}$$

$$G_Y(x) = [B(x) \otimes B_Y^+] - [B(x) \otimes B_Y^-]. \tag{11}$$

Notably, the binary convolution is carried out based on the system illustrated in Fig. 5(a) or Fig. 5(b) using all-optical method, while other values are computed offline. Together, Eqs. (7) to (11) provide a complete computational framework for extracting image gradients and obtaining the final edge detection output.

Results

Basic nonlinear-induced dynamics of a wavelength-multiplexed ADMRR

Figures 6 and 7 present the nonlinear-induced neural dynamics of all-optical spiking neurons based on wavelength-multiplexed ADMRRs, and the spiking neuron exhibit neuron-like self-pulsation, excitability, inhibitory, and cascade behavior under varying conditions. Notably, our proposed wavelength-multiplexed ADMRR-based spiking neurons are consistent with previous phase plane analyses of SOI MRR-based spiking neurons, characterized by a subcritical Andronov-Hopf bifurcation, and classified as Class II excitability[37,41]. Figure 6(a) shows the simultaneous self-pulsation behavior of the ADMRR induced by two pump lasers with distinct resonant wavelengths, injected into the 'Input' and 'Through' ports at equal power (3 mW) and with identical detuning (−20 pm). By increasing the pump power of λ_1 light to 5 mW and decreasing the pump power of λ_2 light to 0 mW, only the self-pulsation behavior of λ_1 light constant presence but the self-pulsation behavior of λ_2 light disappeared, as shown in Fig. 6(b). This demonstrates that each resonant wavelength of the passive ADMRR

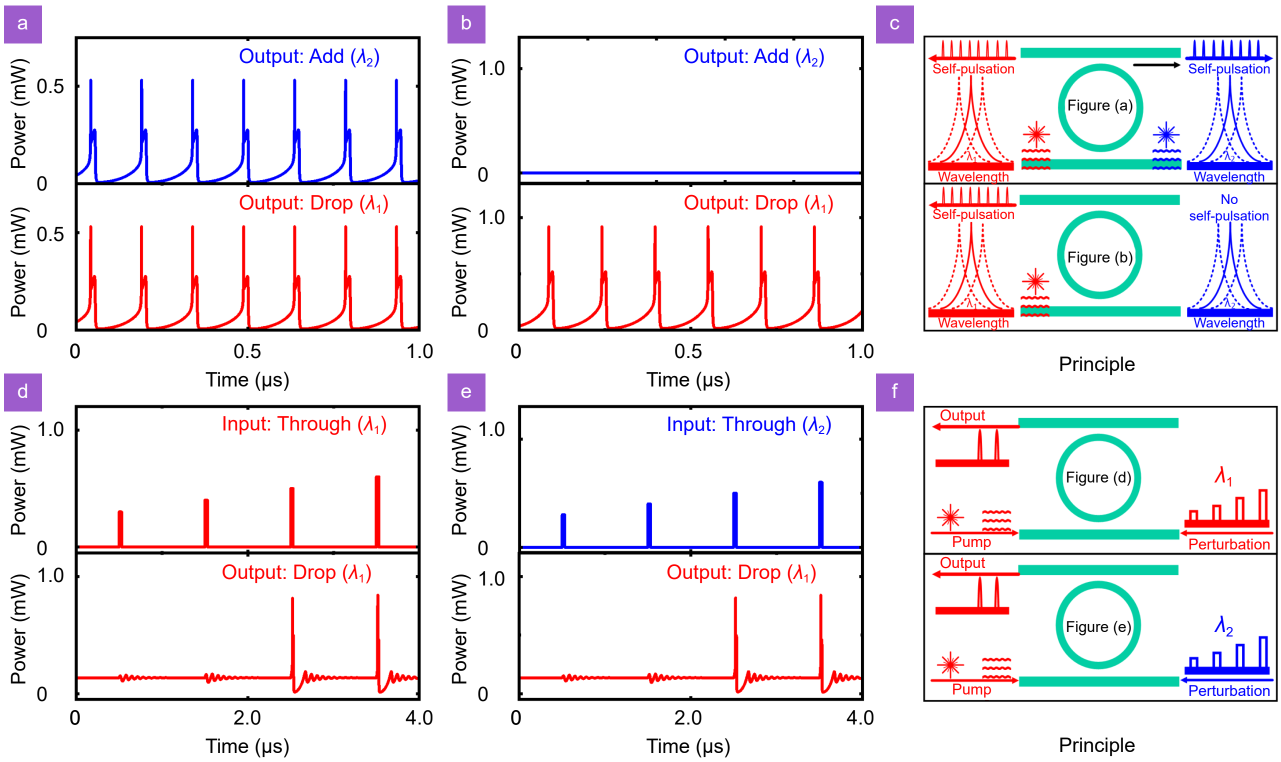

Fig. 6 | (**a**, **b**) Self-pulsation behavior under (a) dual-pump and (b) single-pump excitation. (c) Operating principles corresponding to (a) and (b). (**d**, **e**) Excitability behavior under perturbations at the (d) same and (e) different wavelengths as the pump. (**f**) Operating principles corresponding to (d) and (e).

can independently support periodic thermal-optic oscillations—and thus neural spiking output—if sufficiently pumped. The nonlinear dynamics of the ADMRR continue to induce red- and blue-shifts across the full resonance set, but spiking only occurs at resonances receiving external optical excitation. Subsequently, the power of the λ_1 laser continues to be reduced below the threshold of the self-pulsation, as shown in Fig. 6(d) and 6(e), the self-pulsation behavior disappeared and the spiking neuron stabilized. To probe the excitability, a series of perturbation pulses (30 ns duration) are injected into the 'Through' port at λ_1 and λ_2, respectively. In Fig. 6(d), four perturbation pulses, each spaced by 1 μs, are applied sequentially at λ_1, with the peak power increasing progressively. Similarly, in Fig. 6(e), the same perturbation signal is applied, with the peak power also increasing over time. Figure 6(d) and 6(e) demonstrate that spiking responses are triggered only when the peak power of the perturbation pulses exceeds a critical threshold at each respective wavelength. These results indicate that, following subthreshold suppression of spontaneous oscillations, the system remains quiescent until externally driven across the excitability threshold. Upon sufficient perturbation, the ADMRR undergoes a nonlinear bifurcation-like transition from the resting state to a transient oscillatory trajectory, thereby emitting a single spike. This excitability behavior constitutes a fundamental dynamic feature for implementing neuromorphic digital logic operations.

Moreover, the inhibitory dynamics and cascading behavior of ADMRR-based spiking neuron are demonstrated. As shown in Fig. 7(a) and 7(b), following the generation of a spike, the ADMRR-based spiking neuron enters a refractory period during which it becomes temporarily unresponsive to subsequent perturbations. This refractory phase persists until the system relaxes back to its stable resting state. At the 'Through' port, perturbation pulses exceeding the spiking response power threshold elicit an excitatory behavior of 'Drop' port. Subsequently, a delayed pulse passes through the 'Through' port and is confined within the refractory period of the previous excitatory behavior, thereby effectively suppressing the spiking response of the delayed pulse at both the 'Drop' and 'Add' ports. This observation confirms the presence of a delay-induced inhibition mechanism, which plays a crucial role in shaping the temporal dynamics and logical selectivity of the proposed spiking neurons.

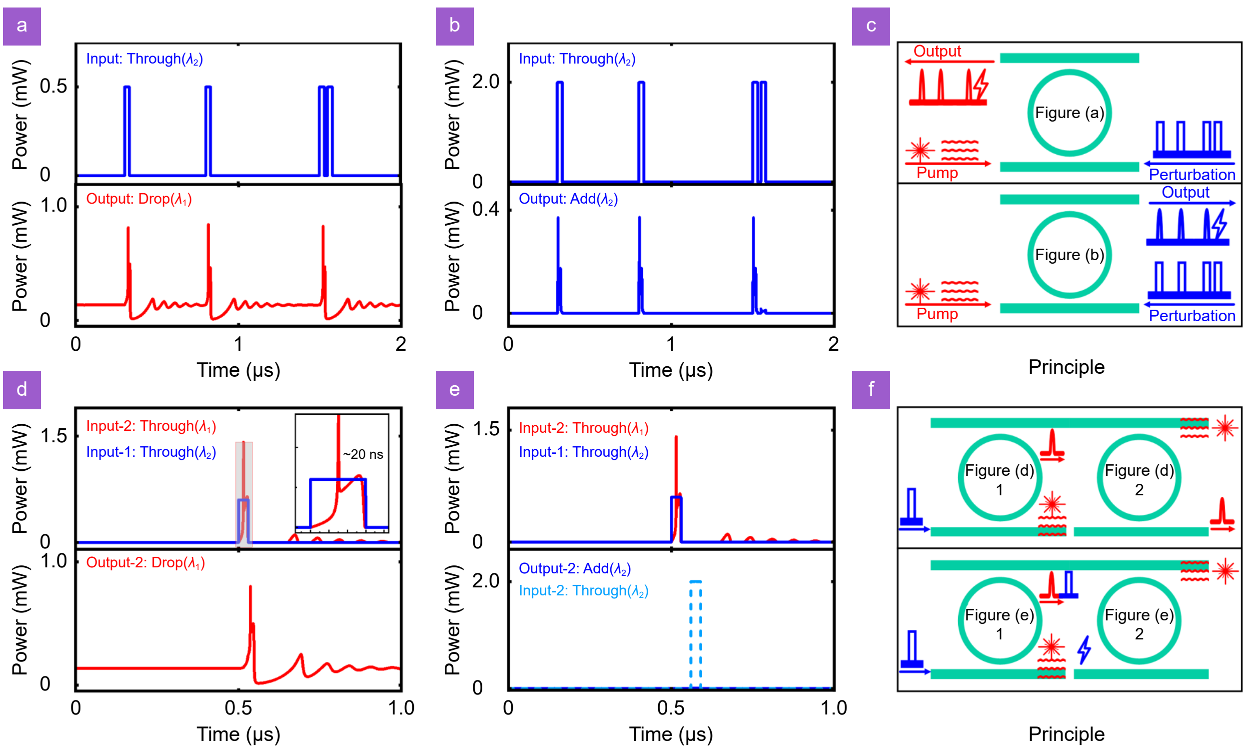

Fig. 7 | (**a**, **b**) Inhibitory responses at the (a) 'Drop' port and (b) 'Add' port under perturbation pulses injected from the 'Through' port. (**c**) Operating principles corresponding to (a) and (b). (**d**, **e**) Demonstration of cascaded (d) excitatory and (e) inhibitory dynamics. (**f**) Operating principles corresponding to (d) and (e).

Next, the cascading behavior of spiking neurons is quite critical to build multi-layer networks for complicated optical computing. To emulate this behavior, two identical ADMRRs are cascaded under the same operational conditions. In practical implementations, it is crucial to apply appropriate spike management—such as attenuation, amplification, or temporal alignment —between successive ADMRR-based neurons to ensure effective signal propagation and functional integrity across layers. As shown in Fig. 6(d), a perturbation pulse is applied exclusively to the first ADMRR, and its generated spike is subsequently processed through spike management before being injected into the second ADMRR-based neuron. Subsequently, the physical parameters of the second ADMRR, including the mode-averaged energy in the cavity, the temperature differential to the surroundings, and the free carrier concentration, evolve similarly to those of the first ADMRR after a certain latency. Consequently, the cascading excitation occurs, where a single spike is observed at the output of the second ADMRR. Furthermore, Fig. 6(e) illustrates cascading inhibition in two cascaded ADMRRs. A perturbation pulse is applied to the first ADMRR to induce a spike, which, after spike management, is injected into the second ADMRR. Meanwhile, a delayed perturbation pulse, differing in wavelength from the first-stage spike, is injected. Subsequently, the input pulse to the second ADMRR is fully suppressed, showing the cascading inhibitory effects of the wavelength-multiplexed ADMRR-based spiking neurons. Overall, the cascaded excitatory and inhibitory dynamics form the theoretical basis for constructing ADMRR-based photonic digital neuromorphic networks.

Results of all-optical digital logic operation

Figures 8 and 9 illustrate the performance of single-layer and dual-layer all-optical digital logic gates, respectively, realized using ADMRR-based spiking neurons. In Fig. 8(a1), the AND operation of ADMRR-based spiking neurons is performed using the excitability threshold mechanism. Two wavelength-multiplexed optical perturbation pulses are injected into the 'Through' port of the ADMRR, each representing a binary input. When the input logic is '1', a perturbation pulse, slightly above half the threshold power but below the full threshold, is injected into the ADMRR. A neural spike is output at the 'Drop' port, indicating a logic '1', only when both input logics corresponding to the different wavelengths are '1'. Otherwise, the output is '0'. Similarly, Fig. 8(a2) shows the OR gate, where a rectangular pulse slightly above the threshold power is injected when the logic is '1'. The 'Drop' port will output a neural spike (logic '1') unless both input logics are '0', in which case the output is '0'. Fig. 8(a3) demonstrates the NOT operation using the inhibitory mechanism. Two perturbation signals of different wavelengths are input through the 'Through' port, with the λ_2 pulse delayed by a time τ relative to the λ_1 pulse (within the refractory period). When the input logic is '0', the λ_1 perturbation is absent, allowing the subsequent λ_2 pulse to elicit a spiking response at the 'Add' port, corresponding to a logic '1'. Moreover, Fig. 8(b1–b3) illustrate photonic crystal-based AND, OR, and NOT gates, realized via nonlinear optical excitatory and inhibitory dynamics, consistent with ADMRR-based logic mechanisms.

Moreover, A single ADMRR can realize complex XOR and XNOR logic operations in a single step by injecting two wavelength-multiplexed perturbation pulses through the 'Through' port, configured according to specific temporal encoding rules. It is worth noting that although XOR and XNOR operations can be directly realized in a single step using an ADMRR with temporally encoded wavelength-multiplexed inputs, these functions can alternatively be constructed through multi-layer cascading of basic logic gates such as AND, OR, and NOT. Figure 8(c) demonstrates the proposed XNOR operation based on the threshold mechanism combined with a temporally encoded input strategy. Four input patterns ('00', '01', '10', and '11') are considered, yielding corresponding XNOR outputs of '1', '0', '0', and '1', respectively, within a time window (T_{window}) of 1 μs. For input pattern '0', a 30 ns pulse with 0.3 mW power is encoded at 0.25 μs within the T_{window} interval; for pattern '1', it is encoded at 0.75 μs. When the two encoded pulses from the 'Through' ports overlap within the same sub-window ('00' or '11'), their cumulative power exceeds the threshold, eliciting a spiking response at the 'Drop' port, corresponding to output '1'. If the pulses do not overlap ('01' or '10'), no spike occurs, resulting in output '0'. Contrastively, Fig. 8(d) illustrates the XOR operation based on inhibitory dynamics combined with a temporally encoded input strategy. For input pattern '0' of λ_1, a 30 ns pulse at 0.6 mW is encoded at 0.25 μs, and for pattern '1', it is encoded at 0.75 μs. While, for λ_2, input pattern '0' is encoded as a 30 ns pulse at 2 mW at 0.28 μs, and input pattern '1' is encoded at 0.78 μs. When the encoded pulses coincide

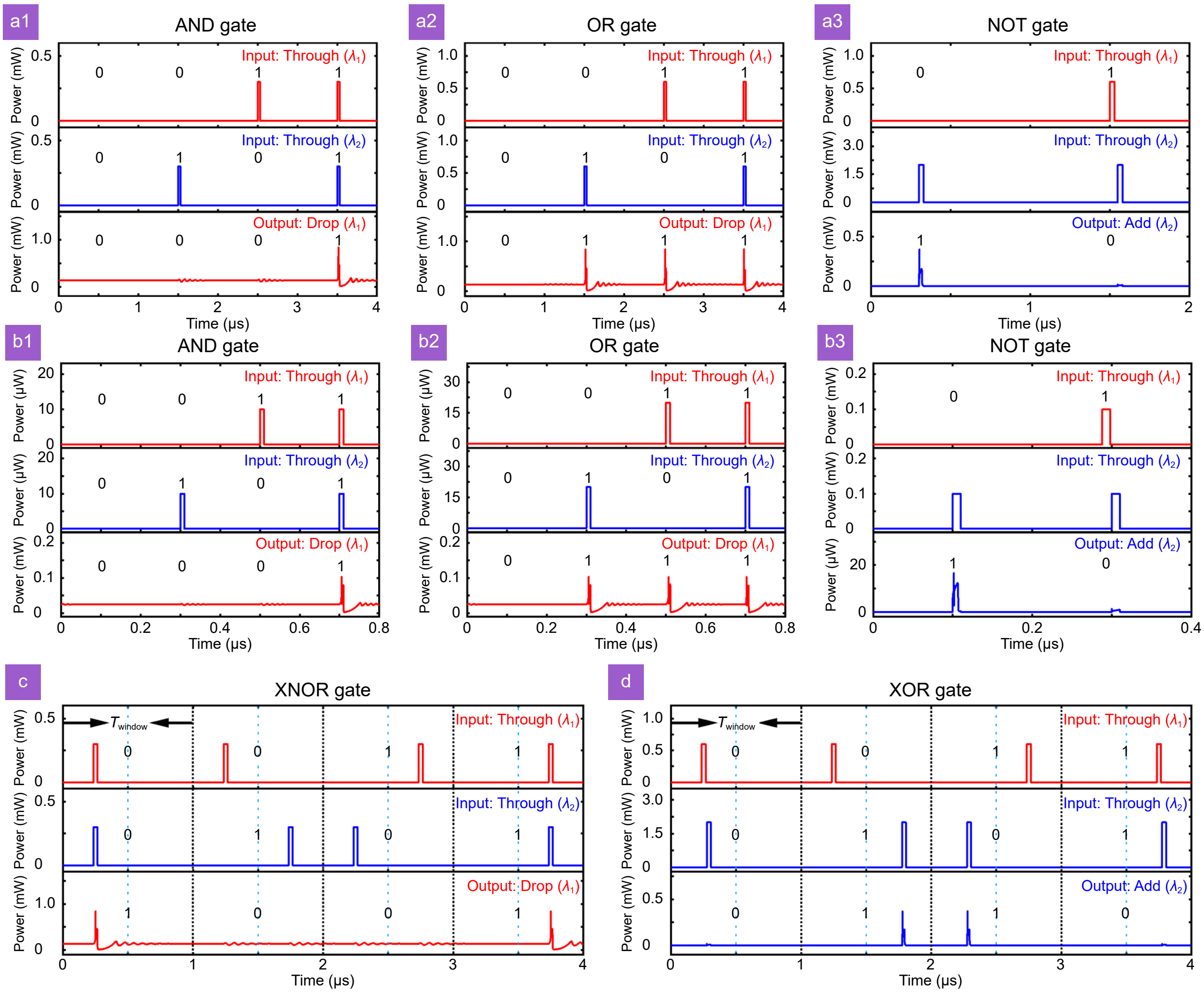

Fig. 8 | Single-layer optical digital logic operations of (**a1**) AND, (**a2**) OR, (**a3**) NOT, (**c**) XNOR, and (**d**) XOR by utilizing ADMRR-based spiking neurons. (**b1**–**b3**) Single-layer optical (**b1**) AND, (**b2**) OR, and (**b3**) NOT gates by using photonic crystal-based spiking neurons.

within the same sub-window ('00' or '11'), the input pulse of λ_1 inhibits spiking at the 'Add' port, leading to no spike and output '0'. However, when the pulses do not coincide ('01' or '10'), the pulses trigger independent spikes at their respective ports, with the perturbation of λ_2 triggering a spike at the 'Add' port, resulting in output '1'.

Subsequently, the implementation of a 4-input AND gate, as well as NAND and NOR logic functions, is realized via a dual-layer cascaded architecture of ADMRR-based photonic logic gates. Figure 9(a1) and 9(a2) show the input-output operation process of the two AND gates in the first layer, with their outputs serving as inputs to the AND gate in the second layer. In Fig. 9(a3), the outputs from the first-layer AND gates are first processed through spike management and subsequently injected into the second-layer AND gate, and the resulting output demonstrates the successful execution of a 4-input AND operation using three cascaded ADMRR-based spiking neurons. Next, Fig. 9(b) illustrates the complete operation and results of a cascaded configuration consisting of a first-layer AND gate and a second-layer NOT gate. For the first-layer AND gates, the input combinations '00', '01', '10', and '11' result in outputs of '0', '0', '0', and '1', respectively. The output spikes from the first layer after undergoing spike management is then routed to the second-layer NOT gate. A rectangular pulse, with a wavelength distinct from the first-layer spike, is injected into the 'Through' port with a specific time delay. A spike is subsequently produced at the 'Add' port of the NOT gate, corresponding to the wavelength of the rectangular pulse. The final outputs are '1', '1', '1', and '0', representing a NAND logic operation. Similarly, Fig. 8(c) shows

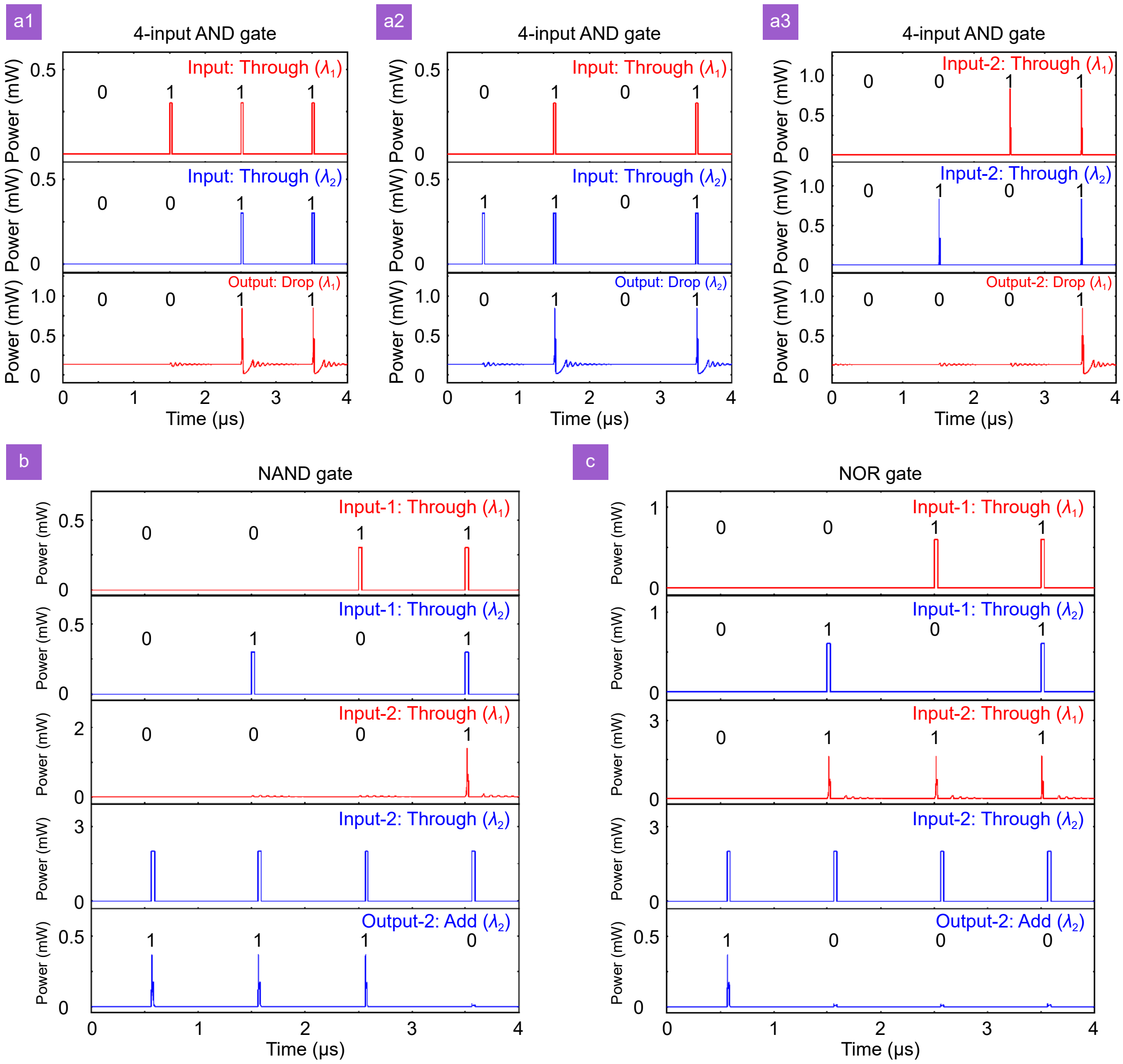

Fig. 9 | Dual-layer all-optical digital logic operations of (**a1**–**a3**) 4-input AND, (**b**) NAND, and (**c**) NOR gate.

the process and results of a cascaded configuration comprising a first-stage OR gate and a second-stage NOT gate. The inputs to the OR gate are '00', '01', '10', and '11', producing output results of '0', '1', '1', and '1', respectively. The output pulse from the first stage is fed into the second-stage NOT gate. A rectangular pulse, with a different wavelength from the first-stage spike, is injected into the 'Through' port with an appropriate time delay. A spike at the 'Add' port, matching the wavelength of the rectangular pulse, results in outputs of '1', '0', '0', and '0', corresponding to a NOR logic operation.

Figure 10 presents the results of complex logic operations enabled by ADMRR-based neurons, demonstrating the feasibility of complex combinational logic based on multi-input logic gate integration. Figure 10(a1) and 10(a2) illustrate the input-output responses of two 4-input AND gates, with each input encoded via wavelength-multiplexed perturbation pulses. A logic '1' is defined by the presence of a pulse at the assigned wavelength, and logic '0' by its absence. To implement AND logic, each perturbation pulse is set to 1/4 to 1/3 of the firing threshold of the ADMRR-based neuron, such that only the simultaneous arrival of all four inputs accumulates sufficient energy at the 'Drop' port to trigger an output spike (logic '1'). Figure 10(a3) illustrates a cascaded 8-input AND gate, where the outputs of two first-layer 4-input AND gates are fed into a second-layer 2-input AND gate. A logic '1' is generated only when all optical perturbations are inputted, validating the correct implementation of 8-input AND logic. Furthermore, Fig. 10(b1)

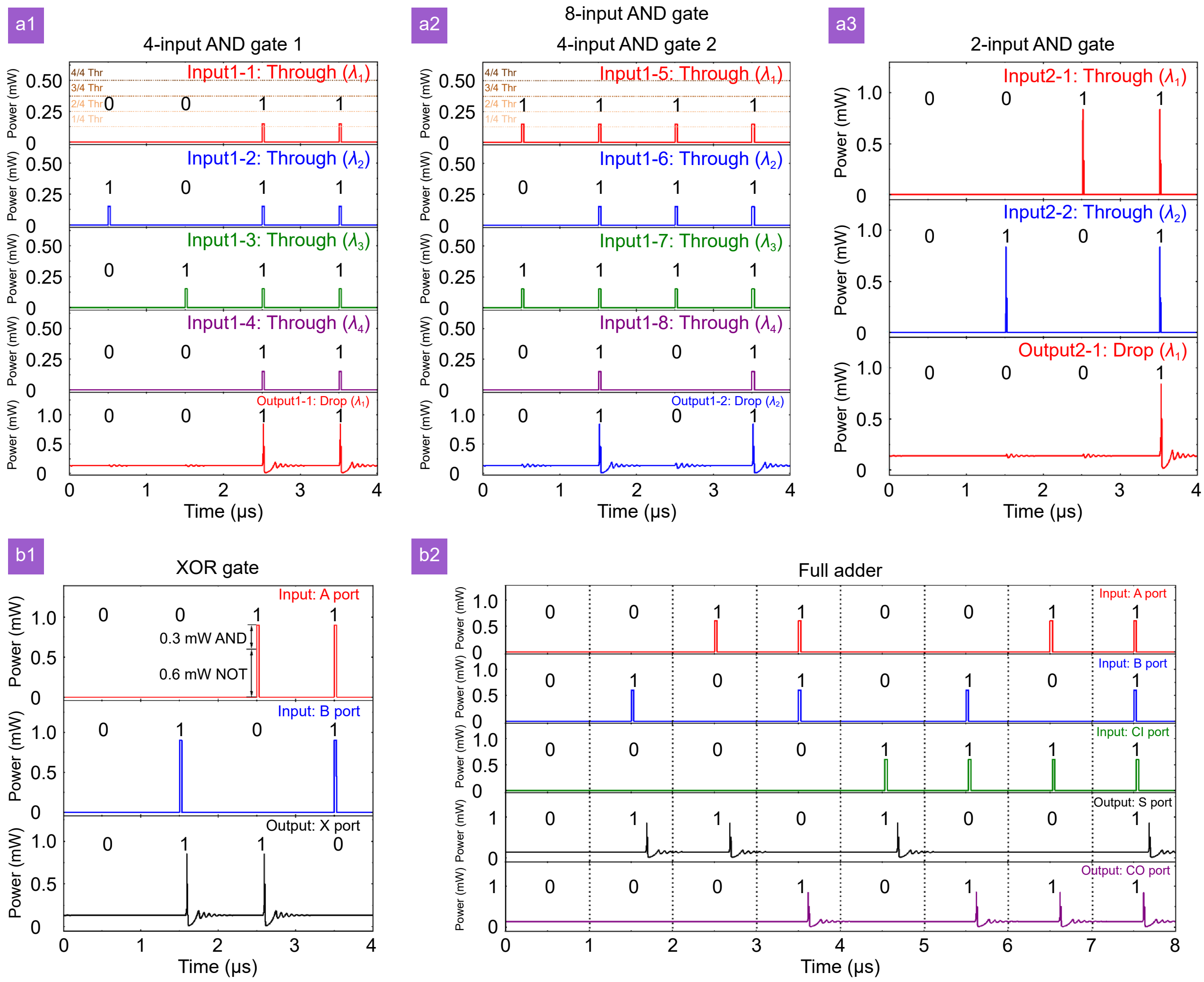

Fig. 10 | Results of multi-layer digital logic operations, including (**a1–a3**) 8-input AND gate, and (**b1–b2**) full adder.

illustrates the implementation of the XOR logic gate based on the configuration shown in Fig. 4(c). The XOR operation is realized by combining two NOT gates, two AND gates, and one OR gate, with each logic stage receiving pulse inputs in accordance with its respective encoding scheme. This ultimately enables the nonlinear discrimination of XOR logic, providing one of the key foundations for the implementation of a full adder. Subsequently, as depicted in Fig. 10(b2), a complete three-input full adder is constructed by combining XOR with AND/OR logic, incorporating input terminals A, B, and carry input CI. Leveraging the excitatory and delayed inhibitory properties of ADMRR pulse neurons, parallel optical execution of XOR, AND, and OR operations is achieved, with the accurate generation of sum (S) and carry output (CO) pulses at the output. All input combinations yield correct results, validating the capability of ADMRR neurons to implement a full adder and demonstrating the feasibility of complex multi-layer digital logic.

Results of all-optical binary convolution and image edge detection based on ADMRRs

Building on the principles in Fig. 5, this section presents the numerical results of ADMRRs-based SNN applied to all-optical binary convolution and image edge detection. Specifically, Fig. 11(a) and 11(b) illustrate representative results corresponding to the two binary convolution schemes based on TDM and WDM, as depicted in Fig. 5(a) and 5(b), respectively. In Fig. 11(a), the TDM-based scheme is demonstrated. Each element of the image and the kernel is encoded in a time window t_i of 0.5 μs, with the image elements assigned to light at resonant wavelength λ_1 and the kernel elements to light at wavelength λ_2. Elements with a value of '1' are represented by rectangular pulses with a power of 0.5 mW and a duration of 10 ns, while elements with a value of '0' have no pulse

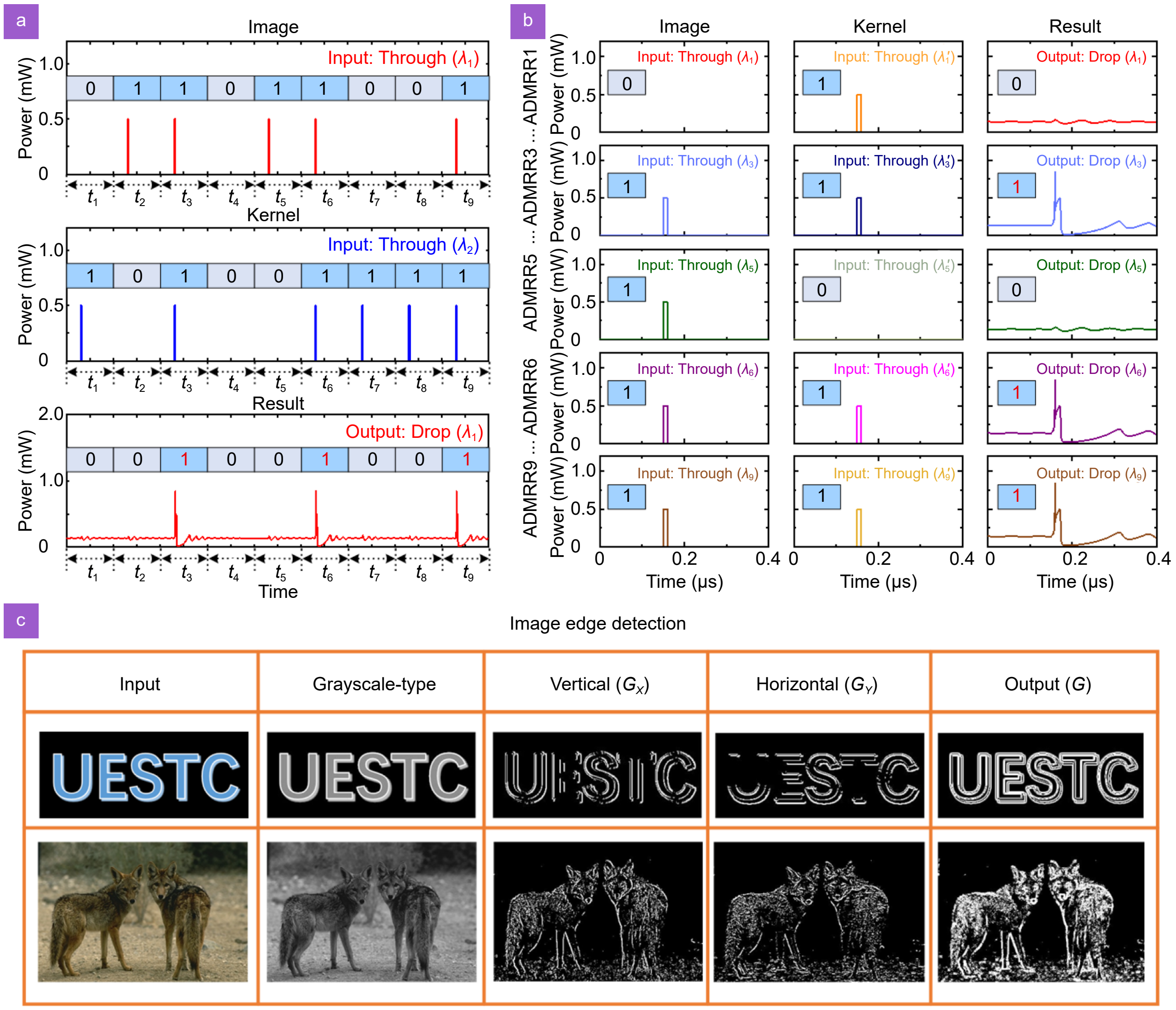

Fig. 11 | Binary convolution operations based on ADMRRs by using (**a**) TDM technology and (**b**) WDM technology. (**c**) "UESTC" and "Wolf" images and their corresponding binary gradient maps.

input. Subsequently, the temporally encoded source image and kernel input signals are simultaneously sent to the ADMRR for an all-optical AND computation. As a result, three excitation spikes are observed at the 'Drop' port of the ADMRR, representing the result of this binary convolution. Figure 11(b) illustrates the WDM-based scheme using a cascaded array of ADMRRs. In this configuration, binary elements of the image and the kernel are respectively encoded onto two distinct resonant wavelengths of each ADMRR in the array. The optical pulse encoding for '1' and '0' remains identical to that used in the TDM scheme. After performing the AND logical operation on the two sets of input signals, the outputs are detected at nine different wavelengths from the 'Drop' port of the cascaded ADMRRs, with three excitation pulses corresponding to the result of the convolution. Notably, this WDM-based approach allows multiple element-wise binary convolution operations to be performed in parallel within a single time window, significantly enhancing processing efficiency.

Figure 11(c) displays the results of an exemplary image edge detection. In particular, each pixel in the preprocessed grayscale image is represented by a 5×5 binary descriptor $B(x)$, which is convolved with four 5×5 kernels: B_X^+, B_X^-, B_Y^+, B_Y^-. These operations yield four results: $B(x)\otimes B_X^+$, $B(x)\otimes B_X^-$, $B(x)\otimes B_Y^+$, and $B(x)\otimes B_Y^-$, where the binary convolution operation is performed using the ADMRR-based all-optical spiking neuron. Subsequently, all $G_X(x)$, $G_Y(x)$, and $G(x)$ are computed offline based on Eqs. (9–11) to reconstruct the edge maps of the image.

The test subjects are an image of the English abbreviation "UESTC" with a resolution of 364×151 pixels and a "wolf" image of with a resolution of 481×321 pixels. Both images are initially converted from color to grayscale during preprocessing. After calculating the gradient for each pixel, the gradient maps of $G(x)$, $G_X(x)$, and $G_Y(x)$ clearly reveal the edge features of these objects. From the results, it can be observed that $G_X(x)$ primarily captures the vertical edge features, while $G_Y(x)$ is more sensitive to horizontal edges. The combined gradient magnitude $G(x)$ effectively integrates both directional responses, yielding a comprehensive edge representation. These findings are consistent with previous studies[22,49].

Here, a quantitative analysis of the energy consumption and computational efficiency of the ADMRR-based system during binary convolution operations is presented. For energy consumption, the energy of a single output spike is ~6 pJ. According to the adopted edge detection method, each pixel requires 4 independent binary convolution operations, corresponding to a total energy consumption of ~144 pJ (6 pJ × 6 × 4). Replacing the ADMRR with a photonic crystal-based device can reduce the energy per pulse to approximately 1 pJ, further lowering the total energy consumption to around 24 pJ. It is worth emphasizing that, since the ADMRR is a passive device, it requires no external electrical driving circuitry, and the static power consumption can be neglected, resulting in a system static additional power consumption of zero. In contrast, conventional electronic processors typically operate within the watt-level power range, while the all-optical ADMRR neurons demonstrate a significant advantage in energy efficiency[50]. In terms of computational efficiency, under the TDM architecture, each binary convolution operation requires 20 ns, resulting in a total processing time of 0.8 μs for four convolutions per pixel (20 ns × 10 × 4). In contrast, with the WDM architecture, convolution operations can be executed in parallel within a single minimal time slot, reducing the per-pixel convolution time to 20 ns, and enabling a system throughput of up to 2 GHz (50 MHz × 40 channels). When utilizing photonic crystal devices, the per-pixel convolution time in the TDM configuration can be further reduced to 0.4 μs, while in the WDM configuration, it can be lowered to 10 ns, leading to an enhancement in system throughput to 4 GHz (100 MHz × 40 channels).

To further demonstrate the accuracy of the proposed binary gradient-based edge detection scheme, a subset of images from the Berkeley Segmentation Dataset (BSDS500) was used for evaluation[51]. Figure 12(a) shows edge confidence maps overlaid with the groundtruth for three methods: binary convolution without pyramid processing, binary convolution with a three-level pyramid scheme, and the conventional Canny's method. In the visualization, orange pixels indicate true positives, while blue pixels represent false positives. To quantitatively assess the detection performance, precision–recall curves are utilized, as shown in Fig. 12(b). It can be observed

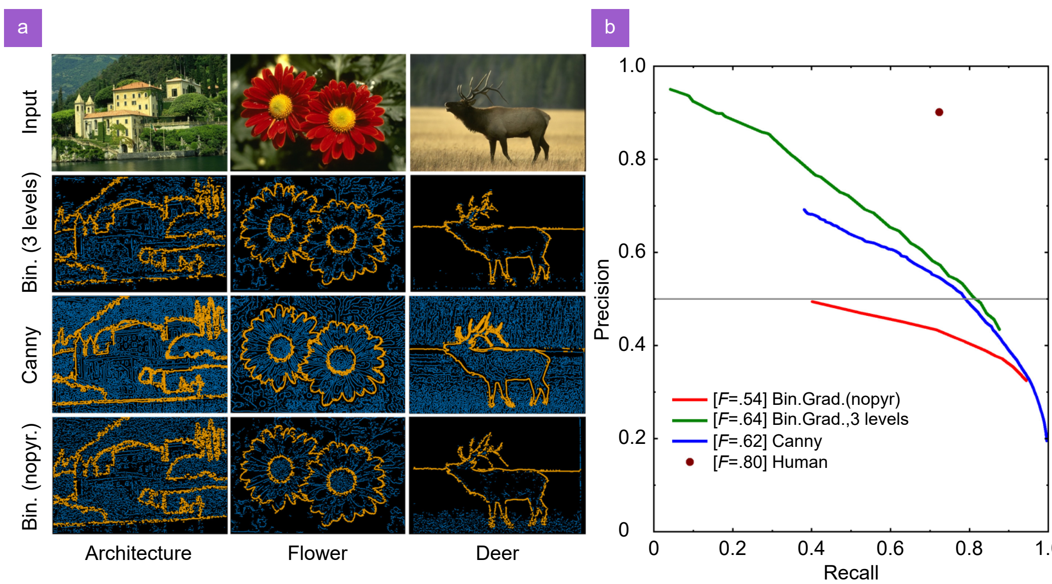

Fig. 12 | (**a**) Visual comparison of edge detection confidence maps overlaid with the groundtruth. (**b**) Edge detection evaluation on the BSDS500 dataset using the binary gradient (Bin. Grad.) method at different pyramid levels, compared to the traditional Canny's method.

that the plain binary convolution method features the simplest structural design but yields lower accuracy compared to the classical Canny's method. However, when enhanced with a three-level pyramid structure, the binary convolution method outperforms the traditional approach in terms of overall performance. This improvement can be attributed to the pyramid's ability to suppress fine-grained noise and effectively reduce spurious responses in textured regions through multi-scale gradient pooling[49]. This confirms that algorithmic refinements enable all-optical binary convolution to achieve accuracy on par with or beyond traditional convolution approaches.

Discussion

The realization of spiking neurons in optical hardware, characterized by ultralow energy consumption, ultrafast processing speeds, and large-scale integration, is a core pursuit in photonic neuromorphic systems. Table 2 provides a comparative summary of performance metrics reported for various photonic spiking neurons. Due to the lack of standardized benchmarks in photonic spiking neuromorphic systems, the values are directly extracted from prior literature as a basis for preliminary assessment. The proposed multi-wavelength auxiliary and competition approach enhances the parallel processing capabilities of both ADMRR-based and other optical spiking neurons. The advantages of multi-wavelength auxiliary and competition scheme in optical spiking neurons from various perspectives are now elaborated below.

Complexity and scalability. The incoherent multi-wavelength injection scheme in ADMRR-based spiking neurons does not increase the complexity of the neuron device. On the contrary, it eliminates the stringent requirement for phase consistency of perturbations under coherent single-wavelength injected situation, thereby simplifying the overall neuromorphic digital computing systems. Specifically, in digital logic systems constructed from cascaded ADMRR-based spiking neurons, the output spikes of upstream logic gates can participate in downstream operations without requiring strict phase alignment. This feature reduces reliance on peripheral control modules, thereby enhancing the scalability of ADMRR-based digital logic systems. Furthermore, ADMRR-based and crystal-based neuromorphic devices feature among the simplest and the smallest footprints to date, contributing to lower overall complexity in the resulting spiking neurons. Low-complexity spiking neurons built on ADMRRs substantially lower the burden of cascading between units, paving the way for scalable neuromorphic circuit design.

Flexibility and computational dimensionality. By introducing multi-wavelength auxiliary and competition mechanisms into ADMRR-based spiking neurons, their functionality extends from handling single-channel coherent signals to processing multi-channel incoherent optical inputs, thus facilitating their incorporation into incoherent photonics SNNs. In addition, the proposed scheme not only supports multi-wavelength encoding at the input port but also enables decoding and

Table 2 | Comparative analysis of photonic spiking neuron performance[22,27,28,40,52–59].

Category	Complexity	Scalability	Footprint	Speed	Platform	Energy of per spike
FP-SA[27]	High	Low	~1500×300 μm^2	~3.3 GHz	III-V	~7.329 fJ
DFB-SA[28,59]	High	Low	~1500×300 μm^2	~2 GHz	III-V	~19.99 pJ
VCSEL[22]	Medium	Low	~200×200 μm^2	~2 GHz	III-V	~0.750 pJ
Microdisk[52]	Medium	Medium	~25π μm^2	~1 GHz	InAsP-Silicon	~20 fJ
Micropillar[53]	High	Low	~4π μm^2	~2 GHz	III-V	~50 fJ
QD[54]	High	Low	~2 mm (Length)	~150 MHz	III-V	~50 fJ
Graphene laser[55]	High	Medium	~40 μm^2	~4 GHz	InGaAsP-C-Si	~75 pJ
Electric-MRR[56]	Medium	High	~45×35 μm^2	~250 MHz	Silicon	~20 pJ
Graphene-MRR[57]	Medium	Medium	~100 μm^2	~40 GHz	Silicon	~0.7 pJ
SWI-MRR*[40]	Low	Medium	~16×16 μm^2	~50 MHz	Silicon	~6.0 pJ
MWI-MRR* (This work)	Low	High	~16×16 μm^2	~50 MHz	Silicon	~6.0 pJ
SWI-crystal*[40,58]	Low	Medium	~5 μm^3 (Volume)	~100 MHz	Silicon	~1.0 pJ
MWI-crystal* (This work)	Low	High	~5 μm^3 (Volume)	~100 MHz	Silicon	~1.0 pJ

*SWI-MRR represents single-wavelength injected MRR, while MWI-MRR represents multi-wavelength injected MRR. Moreover, the SWI-Crystal represents single-wavelength injected photonic crystal microresonator, while MWI-MRR represents multi-wavelength injected photonic crystal microresonator.

classification based on the output spike wavelengths, further enhancing the functional flexibility and representational capacity of ADMRR-based neurons. Moreover, prior demonstrations in DFB-SA photonic spiking neurons[59] have shown that multi-wavelength injection can enhance parallel signal processing, indicating its potential applicability to broader photonic spiking neuron systems.

Operation speed. In our proposed ADMRR-based spiking neuron, the introduction of a multi-wavelength auxiliary and competition mechanism does not affect the intrinsic information processing speed of the device, with individual spike response times on the order of ~20 ns. Benefiting from the compatibility of ADMRR devices with WDM, parallel arrays of spiking neurons can be constructed, thereby significantly improving the throughput of optical neuromorphic computing systems. Notably, the overall operating speed of the ADMRR-based spiking neuron is primarily limited by the relatively slow resonance wavelength tuning process induced by thermal nonlinear effects. However, by integrating graphene into the MRR waveguide to enhance nonlinear effects, spike information processing rates of up to 40 GHz have been achieved in previous reports under the condition that thermal effects are negligible[57]. As a general solution, the multi-wavelength auxiliary and competition scheme is highly compatible with spiking neurons featuring multiple resonant wavelengths, thus holding significant potential for application in such high-speed spiking neurons.

Energy efficiency. The ADMRR-based spiking neurons are passive devices that require no additional electrical driving power, with static power consumption approximated as zero when not in operation. Here, a preliminary estimation of the power consumption during operation is provided, only considering the output spikes and the applied multi-wavelength perturbation signals. The average power of the output excitatory spike is approximately 0.3 mW, with a pulse width of 20 ns, resulting in an energy of 6 pJ per output spike. The total power of the two rectangular perturbation pulses at different wavelengths reaches 0.6 mW, with a pulse width of 10 ns, resulting in an energy of 6 pJ for the input pulses. Consequently, the estimated energy efficiency of the ADMRR-based spiking neuron is approximately 12 pJ. Moreover, photonic crystal-based spiking neurons are expected to exhibit lower energy consumption and faster processing speeds.

Experimental implementation challenges. The practical implementation may encounter several challenges, including resonance shifts caused by fabrication imperfections, accumulated signal loss in cascaded structures, synchronization of multiple input signals, spiking power management, and precise delay control. These factors may affect the system's stability and scalability. Nevertheless, the proposed structural design is compatible with existing photonic integration platforms, indicating the potential for future experimental demonstration and system-level implementation.

Conclusions

In this work, we proposed and demonstrated a universal and concise hardware architecture designed to perform the neuromorphic digital logic operations by employing wavelength-multiplexed ADMRRs-based spiking neurons. On the one hand, to the best of our knowledge, a universal coupled-mode theory model that incorporates multi-wavelength resonance characteristics, applicable to all side-coupled passive microresonators, is proposed for the first time. The simulation results demonstrated nonlinear-induced neural spiking dynamics, including Class II excitability based on subcritical Andronov-Hopf bifurcation, time-delayed inhibition, and cascaded behavior, enabled by a multi-wavelength auxiliary and competition scheme. On the other hand, single-layer digital logic gates including AND, OR, NOT, XOR and XNOR gate, were demonstrated by employing our proposed encoding rules, and subsequently, building upon these fundamental digital logic gates, complex optical digital logic operations can be implemented with low power consumption through mutual cascading. Moreover, an all-optical binary convolution system using our proposed wavelength-multiplexed ADMRRs-based photonic spiking neurons was proposed as an exemplarity application of neuromorphic digital logic operation to implement image edge detection. In summary, the proposed photonic neuromorphic digital architecture not only does it realize complete optical digital logic operations, but also fosters extensive integration capabilities within the spiking neural network structure. This paves the way for a pragmatic technique in the advancement of photonic neuromorphic systems.

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Author contributions

All the authors analyzed and discussed the results.

Competing interests

The authors declare no competing financial interests.

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