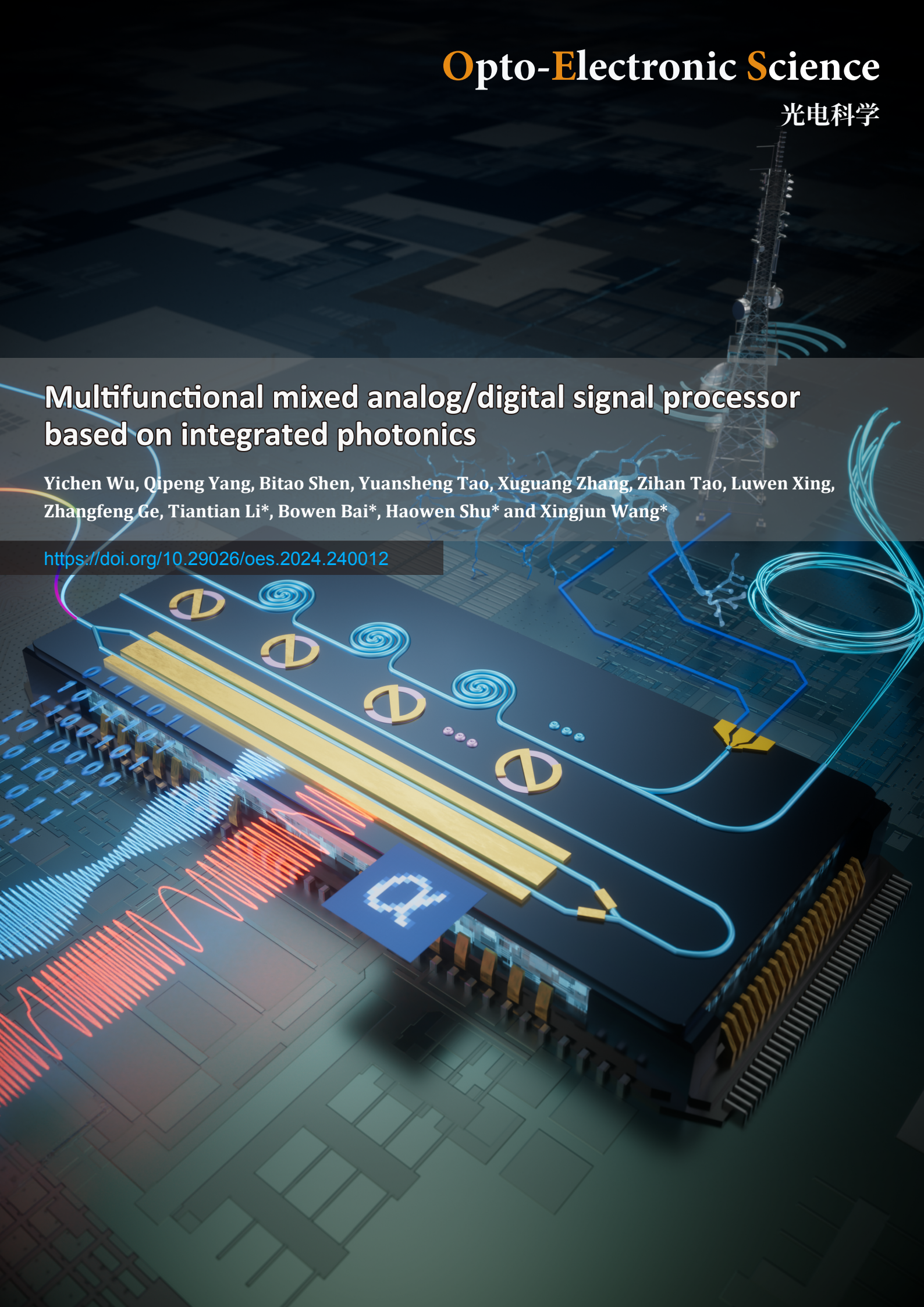


Multifunctional mixed analog/digital signal processor based on integrated photonics

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Multifunctional mixed analog/digital signal processor based on integrated photonics

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Photonic signal processing offers a versatile and promising toolkit for contemporary scenarios ranging from digital optical communication to analog microwave operation. Compared to its electronic counterpart, it eliminates inherent bandwidth limitations and meanwhile exhibits the potential to provide unparalleled scalability and flexibility, particularly through integrated photonics. However, by far the on-chip solutions for optical signal processing are often tailored to specific tasks, which lacks versatility across diverse applications. Here, we propose a streamlined chip-level signal processing architecture that integrates different active and passive building blocks in silicon-on-insulator (SOI) platform with a compact and efficient manner. Comprehensive and in-depth analyses for the architecture are conducted at levels of device, system, and application. Accompanied by appropriate configuring schemes, the photonic circuitry supports loading and processing both analog and digital signals simultaneously. Three distinct tasks are facilitated with one single chip across several mainstream fields, spanning optical computing, microwave photonics, and optical communications. Notably, it has demonstrated competitive performance in functions like image processing, spectrum filtering, and electro-optical bandwidth equalization. Boasting high universality and a compact form factor, the proposed architecture is poised to be instrumental for next-generation functional fusion systems.

Keywords: silicon photonics; multifunctional signal process; microwave photonics; optical computing; optical communication equalization

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Introduction

With the increasing demand for data capacity and processing speed, electric information processing is facing the bottleneck of bandwidth and power consumption¹. A solution to achieve power-efficient and high-speed information processing is to implement information process-

ing in the optical domain^{2,3}. With high-speed electrical-optical-electrical converting devices, both digital data and microwave signals can be loaded to optical carrier and processed directly with specified photonic hardware. This approach potentially offers significant advantages, including unprecedented operational bandwidth and

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reduced delay time. Furthermore, the recently emerged integrated photonic technology presents solutions for enhanced performance in Size, Weight, Power, and Cost (SWaP-C)⁴. To fully harness the inherent superiorities of photonic signal processing, a comprehensive system architecture is needed. Such a system should support multi-dimensional operations on the frequency, amplitude, phase, and time delay of wideband optical signals in a highly integrated form. However, developing a chip-level architecture with high versatility and competitive performance still remains elusive.

The paradigm of application-specific photonic integrated circuits (ASICs) has been the predominant approach in integrated optics for signal processing thus far^{5–7}. Analogous to ASICs in electronic devices, optical components featuring specific combinations are designed for particular applications, such as spectrum filtering^{8–11}, frequency measurement^{12–14}, optical computing^{15–17}, and signal equalization^{18–20}. While this approach offers considerable performance advantages, its universality remains constrained. Another alternative solution is to develop the general-purpose processor architecture called the field programmable photonic gate arrays (FPPGA)^{21–23}. Such generic architectures typically rely on a cascade of 'mesh units' comprising beam splitters or Mach-Zehnder interferometers (MZIs)^{24–26}. With this design, the system response function can be programmed to meet various spectrum processing requirements. Despite their flexible tunability, FPPGAs have so far primarily focused on spectrum filtering tasks mainly in the optical domain experimentally. They are limited in regulating dimensions, handling only phase and amplitude, and currently lack high-speed, on-chip electro-optic (EO) conversion functions. Moreover, the functions achieved often remain rudimentary while the configuration process is complex^{27–29} and the performance is restricted by cumulative errors^{30,31}.

To fully capitalize on the advantages of integrated photonics, a signal processing unit should compromise the following characteristics: Firstly, the chip ought to possess signal loading capabilities, applicable in both analog and digital formats, typically relying on an E/O modulator (array). Secondly, the system should support both coherent and incoherent signal processing. This means processing based on either the principles of spectrum interference or digital signal processing, often through the direct accumulation of orthogonal components like frequency or mode. Moreover, the architec-

ture needs to be as compact as possible to maximize performance per unit area. This includes metrics such as data throughput and processing density, which largely depend on the efficient arrangement of various functional units.

In this paper, we demonstrate a multi-functional and highly reconfigurable monolithic signal processing system based on a silicon-on-insulator (SOI) platform and conduct comprehensive and thorough analyses at the levels of device, system, and application. A cascaded microring resonators and delay lines (CMRR-DL) architecture is proposed and in-depth analyzed for multidimensional optical operations including wavelength selection, amplitude adjustment, and time delay. Additionally, a high-speed silicon modulator is co-integrated for the loading of various signal types. Such a system showcases strong adaptability across different applications. Therefore, as a proof-of-concept verification, the on-chip processor is applied to three different signal-processing scenarios. For microwave processing, it functions as a digital spectrum filter with high main-to-sidelobe suppression ratio and tunable 3 dB bandwidth. In data transmission, it acts as a signal equalizer for bandwidth extension via frequency interference management. More complexly, this processing chip can accelerate matrix calculation operations in image processing, offering unprecedented speed and precision (9 bits). The results demonstrate that the proposed system combines the excellent specialized performance characteristic of the ASIC architecture with the flexible reconfigurability of the FPPGA architecture. This synergy provides a novel approach to constructing multi-functional, on-chip information processing systems.

System architecture and principle

The architecture of the proposed system is illustrated in Fig. 1(a). The monolithic system is fabricated on SOI platform, occupying a compact footprint of approximately 2.6 mm², as shown in Fig. 1(b). At the input, a wide-bandwidth Mach-Zehnder modulator (MZM) loads electrical information into the optical domain. Subsequently, the CMRR-DL composed of an alternating array of microring resonators (MRRs) and waveguide delay lines is arranged to process and reshape the modulated signals. Individual MRR can be precisely tuned to switch and weight optical signals at selected wavelengths to the drop ports, by adjusting applied voltage to corresponding micro-heaters. The waveguide

delay lines are inserted between MRRs with the same delay time, matching the signal bitrate under processing or the needed group velocity dispersion (GVD) among channels of varying wavelengths. As different signals pass through the system, the equidifferent delay will be applied, wherein signals filtered by the first (last) MRR experiencing no delay (pass through all delay lines). This dynamic tuning results in distinct optical transmission properties at both the through and the drop ports, including amplitude, phase and delay time on arbitrary wavelength channels via different micro-heater voltage setups, thereby facilitating a range of multifunctional operations. Additionally, the CMRR-DL system can function as either a coherent or incoherent architecture according to the signal carrier form and perform analog or digital signal processing.

For an input signal with monochromatic light carrier, the chip acts as a coherent processor and can process both analog and digital signals. In the analog mode, the spectrum response around the target wavelength results from the interference among different channels. Within each channel, there lies a tunable add-drop MRR, which facilitates amplitude and phase tuning prior to interference, therefore programming the final spectrum response coherently. The ability to produce diverse optical

spectral shapes and subsequently generate varied Ratio-Frequency (RF) responses, is instrumental in optical communication, which can be utilized to improve the bandwidth of the communication system as a frequency domain equalizer. In the digital mode, the chip has the potential to function as a time domain equalizer, also known as a feed forward equalizer (FFE). Based on the discrete tapped delay line (TDL) architecture, the transmission of signals with different delay time can be adjusted by tuning the MRRs, and the tapped signals are combined at the drop port. The recombination of signals can effectively compensate for the channel distortion, such as inter-symbol interference (ISI) caused by the dispersion within the communication link. The brief principles of both procedures are illustrated in Fig. 1(c–e), with signals (i–v) of Fig. 1(d) and 1(e) representing the signals in the corresponding position of Fig. 1(c). In Fig. 1(d) depicting the frequency domain equalization, (i) represents the base-band electrical signal with ideal frequency spectrum, (ii) illustrates the modulated signal spectrum with inconsistent RF loss and (iii) showcases the compensated spectrum with a flat shape. In Fig. 1(e) of the time domain equalization, the red lines denote the original signal with interferences existing at the sampling points, while the blue lines refer to the signal after

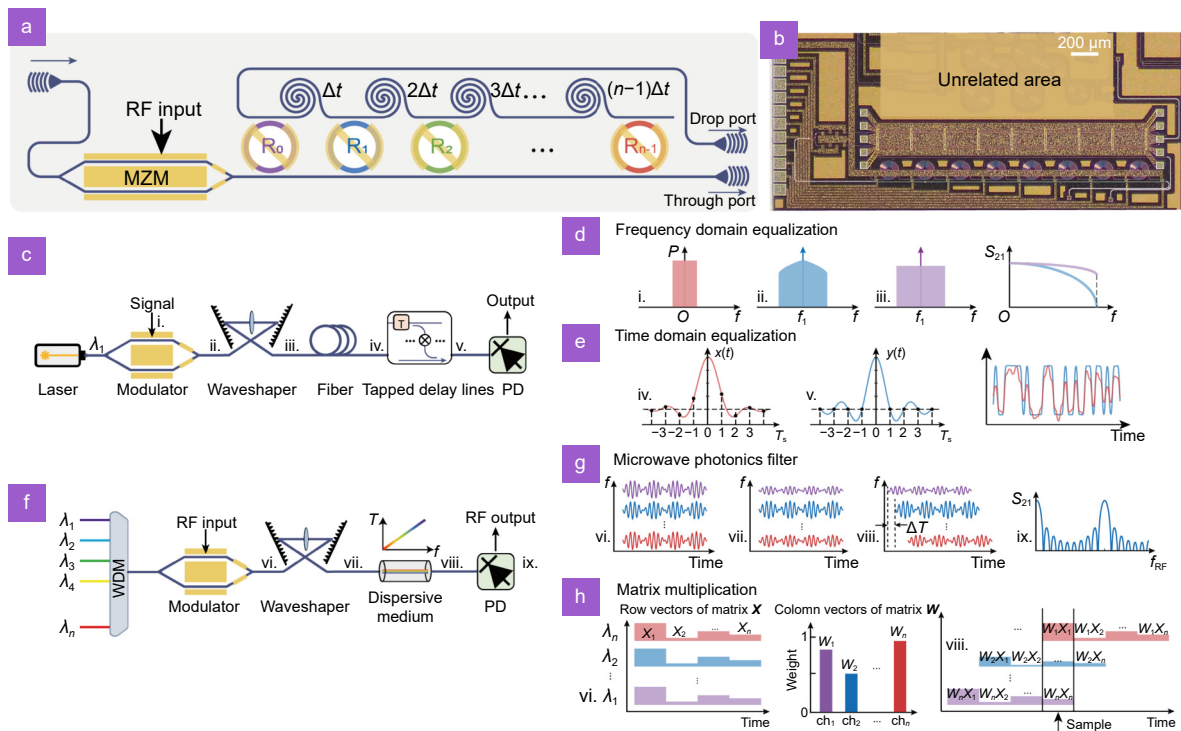


Fig. 1 | Integrated multi-functional information processor based on CMRR-DL. (a) The schematic of the chip layout. (b) Optical microscope image of the on-chip system. (c, f) The operational principle of the system as a (c) coherent or (f) incoherent architecture displayed by discrete devices. (d, e, g, h) Signals flow charts when applied in fields of (d, e) optical communication, (g) microwave photonics and (h) optical computing.

equalization, where the ISI has been mitigated by the TDL structure. The detailed equations about the equalizer are shown in Supplementary information Section 1. The effectiveness as a frequency domain equalizer is shown in “Application demonstration” section, whereas the performance as a time domain equalizer will be explored in the future work.

For multi-wavelength input, after the signal loading, the parallel optical carriers are modulated with the same signal $S_i(t)$. The optical transmission property of MRRs is adjusted to match the expected transmission spectrum denoted as $T(\lambda_i)$. Meanwhile, the CMRR-DL serves as an on-chip discrete dispersive medium, where light at different wavelengths is guided to various optical paths with stepped-increasing delay time. Then the multi-wavelength optical signals from CMRR-DL are detected by a PD where light intensity for each channel is summed. The detected RF signal can be expressed as:

$$S_o(t) = \sum_{i=0}^{N-1} A_0(\lambda_i) T(\lambda_i) S_i(t - i\tau), \quad (1)$$

where $A_0(\lambda_i)$ is the optical carrier intensity, τ is the fixed discrete delay time of waveguide delay lines, N is the number of used channels and wavelength. This expression neglects the cross-talks between channels when the channel spacing and extinction ratio are high enough, which is discussed in Supplementary information Section 3. As an incoherent architecture, the CMRR-DL system can be leveraged to implement distinct applications.

One is a digital filter based on the principle of finite-impulse response (FIR)^{32–34}. The CMRR-DL system serves as a multi-wavelength TDL architecture. As illustrated in Fig.1(g), given the relationship between input RF signal $S_i(t)$ and output RF signal $S_o(t)$ expressed in Eq. (2), the transfer function in the frequency domain of the FIR filter can be formulated as:

$$\begin{aligned} H(\omega) &= \frac{S_o(j\omega)}{S_i(j\omega)} = \frac{\sum_{i=0}^{N-1} A_0(\lambda_i) T(\lambda_i) e^{-j\omega\tau} S_i(j\omega)}{S_i(j\omega)} \\ &= \sum_{i=0}^{N-1} A_0(\lambda_i) T(\lambda_i) e^{-j\omega\tau}, \end{aligned} \quad (2)$$

where ω is the RF angular frequency and $A_0(\lambda_i) T(\lambda_i)$ is the tap coefficient. The signals in positions (vi-ix) of Fig. 1(f) are depicted in Fig. 1(g). Notably, a periodic frequency response is demonstrated with the parameter set of $N = 8$, $\tau = 100$ ps, and $A_0(\lambda_i) T(\lambda_i) = 1$.

The other is to perform optical positive matrix multiplication based on a time-wavelength plane stretching approach^{35–37} as shown in Fig. 1(h). In this process, the column vectors $\mathbf{x}^T$ of matrix $\mathbf{X}$ are temporally transformed into $S(t)$ and subsequently intensity-modulated to optical carriers. Simultaneously, the row vectors $\mathbf{w}$ of matrix $\mathbf{W}$ are mapped to the transmission intensity of MRRs as $A_0(\lambda_i) T(\lambda_i)$. After the time stretching operation implemented by waveguide delay lines, the elements of matrix product $\mathbf{G}$ can be derived by sampling the RF signal within a specific time interval, with the expression $g = \sum_{i=0}^{N-1} w_i x_i$. For matrix multiplication involving negative elements, a straightforward transfer approach is employed which will be further discussed in Section *Application demonstration*.

Device characterization

The multi-function monolithic silicon photonic integrated circuit is fabricated using a standard 90-nm SOI lithography process by a commercial silicon photonics foundry. Figure 2 illustrates the components utilized in the system and their key performance metrics.

The MZM, consisting of a pair of traveling-wave PN junctions, exhibits a >27 GHz 3-dB EO modulation bandwidth (Fig. 2(b)). With a limited number of PRBS15 bits ($n = \lfloor 4 \times 10^5 / (80 \text{ GHz/bitrate}) \rfloor$), error-free back-to-back transmission performance is achieved, showing the bit error rate (BER) lower than $1/n$, as depicted by the red dashed line in Fig. 2(c). Alternatively, the BER can be calculated based on Gaussian statistics³⁸, represented by the blue line in Fig. 2(c). To ensure operation across a wide wavelength range, thermal-optical phase shifters are employed to compensate for phase errors from fabrication.

The tunable MRRs equipped with on-ring TiN micro heaters function as wavelength filters, allowing reconfiguration of the on-chip optical path and adjustment of transmission spectra. The MRRs in the system are designed based on rib waveguides, featuring a rib width of 450 nm and a slab height of 90 nm. Symmetric coupling coefficients are employed, aiming to operate at the nearly critical coupling state to achieve a high extinction ratio. These MRRs demonstrate high tuning efficiency, requiring less than 30 mW of heater power to achieve a 1.6 nm (about 200 GHz) wavelength shift as illustrated in Fig. 2(e), which corresponds to a frequently used wavelength channel interval in various applications.

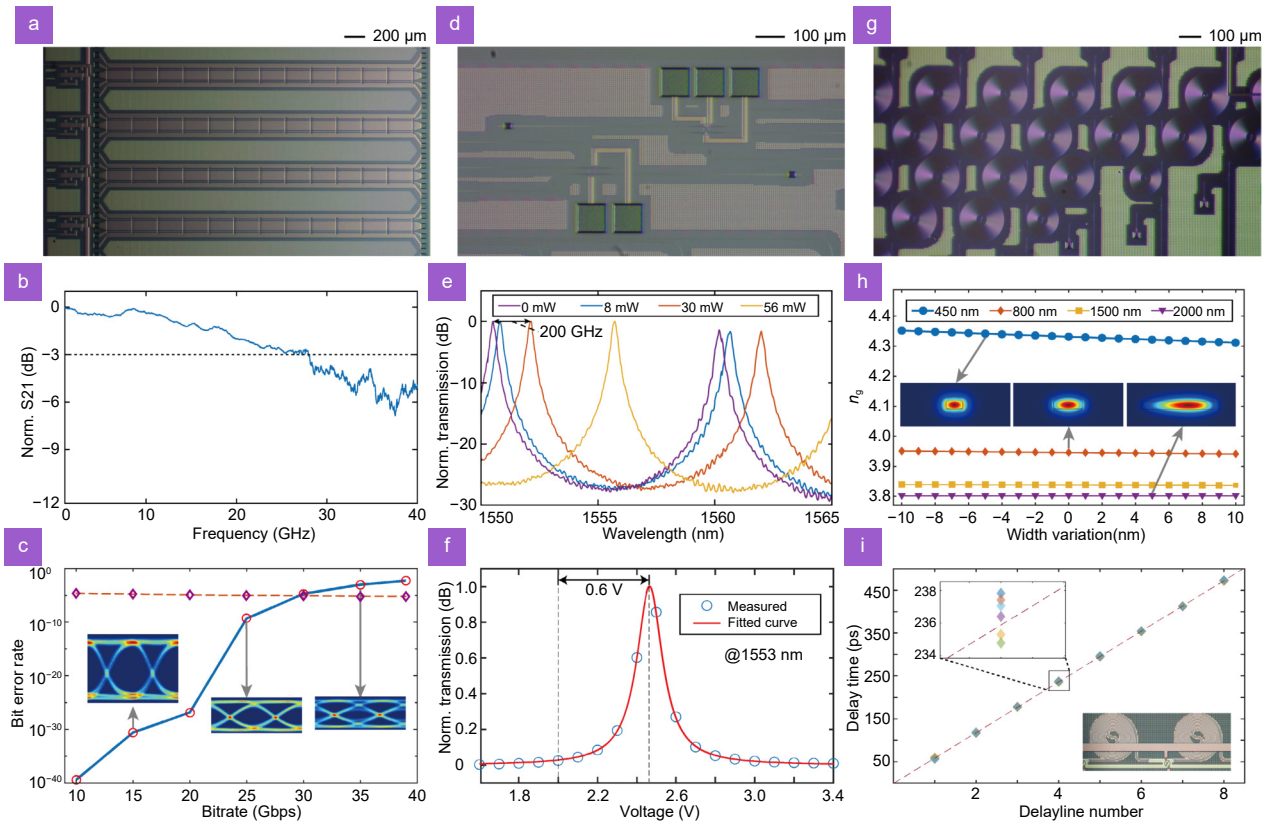


Fig. 2 | Optical images and fundamental characteristics of Si-based devices. (a–c) High-bandwidth silicon MZM. (b) The 3-dB EO bandwidth reaches 27 GHz. (c) The measured BER and eye diagrams versus data rates. (d–f) Tunable MRRs with on-ring TiN heater. (e) Normalized transmission spectra and (f) normalized power at a fixed wavelength versus TiN heater voltages. (g–i) The silicon spiral waveguide delay line. (h) Simulated group refractive index of the fundamental transverse electric (TE) mode versus width variation for various nominal widths. (i) The measured average delay time is 58 ps per spiral waveguide delay line.

Moreover, Fig. 2(f) shows that a mere voltage change of approximately 0.6 V is sufficient to implement a change of the normalized transmission power of the MRR from nearly zero to one at a fixed wavelength.

To achieve on-chip true-time delays with lower loss and less sensitivity to fabrication error, 2-μm wide silicon waveguide spiral is designed with adiabatic bends, featuring an insertion loss of <0.006 dB/ps. Figure 2(h) demonstrates the investigation of sensitivity in group refractive index (n_g) of various waveguide geometries to width variations. Simulated width variations of ± 10 nm show that wider waveguide provides smaller sensitivity to width changes but requires a larger footprint³⁹. Furthermore, the delay time of the spirals employed in the system is measured using the optical vector network analyzer method based on single-sideband modulation (SS-BM-OVNA)⁴⁰. The results indicate an average delay time of 58 ps with a variation of less than 3% (Fig. 2(i)) and the deviation can be further mitigated by introducing tunable delay time structure⁴¹.

System response and optimization

Figure 3 illustrates the passive optical characterization of the CMRR-DL system, along with the summation and multiplication operations. The cascaded MRRs array features an increasing radius, resulting in a free spectral range (FSR) of approximately 11.1 nm and a channel space ($\Delta\lambda_{ch}$) of 0.74 nm, which are slightly different according to the radius. In Fig. 3(a), both the measured and simulated optical spectra of the CMRR-DL are presented. Due to fabrication deviations, overlaps and random wavelength shifting of the MRRs occur, leading to variations in their resonant characteristics. By precisely tuning the heaters on MRRs, the shifting resonant wavelengths of MRRs can be corrected.

By applying different voltages to individual MRRs, the resonant wavelength of each MRR can be tuned distributing uniformly, as depicted in Fig. 3(b). In this configuration, a channel spacing $\Delta\lambda_{ch}$ of 1.2 nm is employed to minimize crosstalk among the nine channels. Due to the propagation loss of waveguide delay lines, the

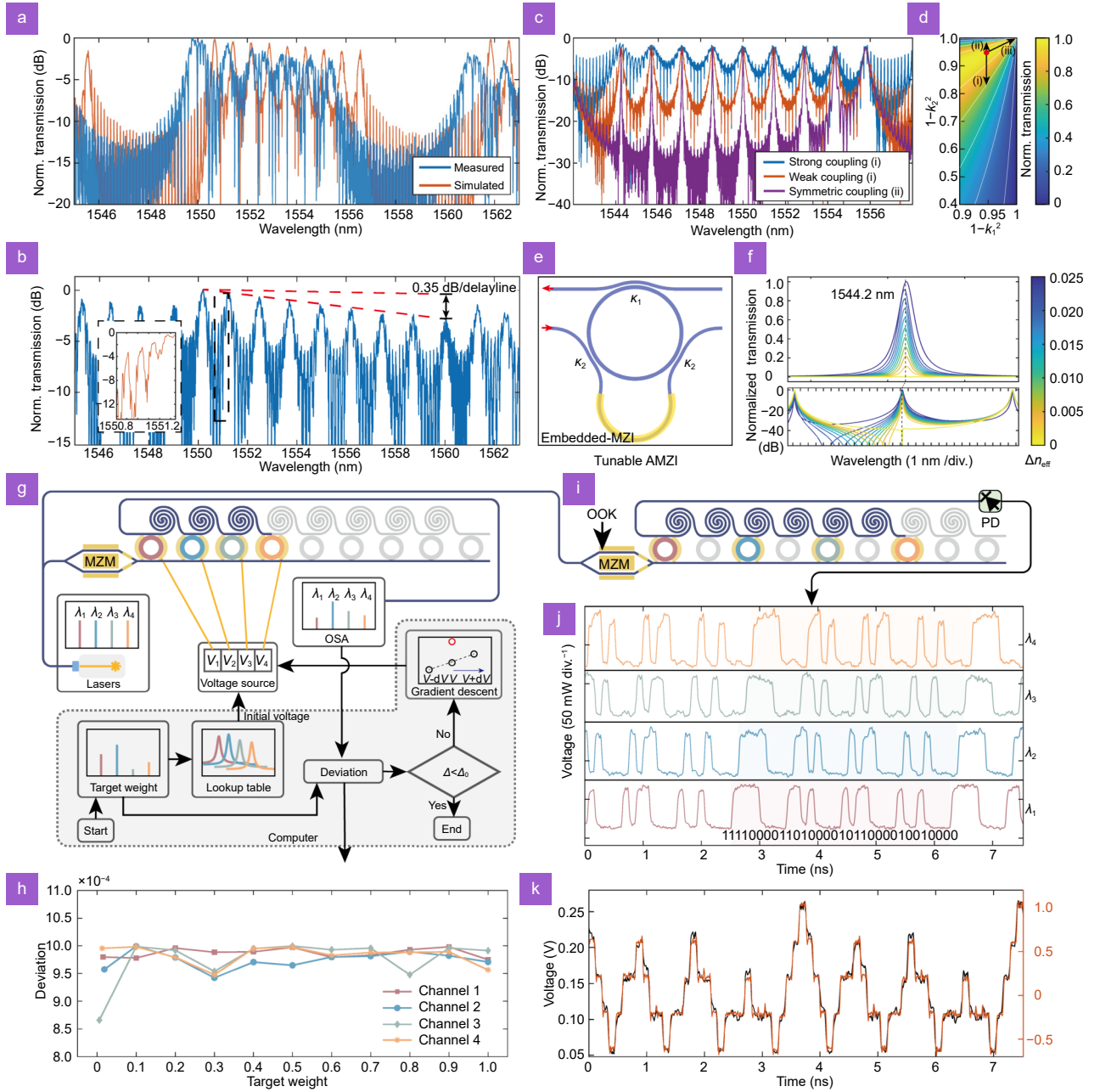


Fig. 3 | Fundamental characteristics at the system level of the CMRR-DL structure. (a) Measured and simulated optical normalized spectra of drop port when heaters are deactivated. (b) Measured spectrum with a particular set of voltages applied to make resonant wavelength of the 9 MRRs distribute uniformly. (c) Flattened peaks of MRRs by adjusting coupling states of MRRs. (d) Normalized transmission versus coupling coefficients of MRR. (e) Structure of MRR with AMZI structure and (f) simulated spectra showing tunable peak power when applying different Δn_{eff} on the AMZI region to simulate the phase shift changing. (g, h) The demonstration of the multiplication operation. (g) Experimental setup and flow chart to set multipliers by gradient descent algorithm. (h) The measured multipliers' deviation. (i-k) The demonstration of summation operation. (i) Experimental setup. (j) Signals propagating through different paths with a bit-period time delay. (k) Measured and simulated summation results in the electric domain.

peak transmission power $T_{\text{drop,max}}$ of each MRR decreases at a rate of 0.35 dB per channel. To mitigate this problem, the coupling state of the MRRs with less delay line propagation loss can be adjusted to realize a lower resonant peak transmission power of the drop port, accord-

ing to the map between the max transmission power of the drop port and the coupling coefficients (κ_1 and κ_2 , $t_1 = \sqrt{1 - \kappa_1^2}$ and $t_2 = \sqrt{1 - \kappa_2^2}$), as shown in Fig. 3(d). Given a target $T_{\text{drop,max}}$, a constant value line can be drawn with various pairs of coupling coefficients and the

shape of the resonator's spectrum depends on the value of $t_1 t_2$. The relationships can be written as follows:⁴²

$$T_{\text{drop,max}} = \frac{(1 - t_1^2)(1 - t_2^2)a}{(1 - t_1 t_2 a)^2}, \quad (3)$$

$$T_d = \frac{(1 - t_1 t_2 a)^2 T_{\text{drop,max}}}{1 - 2t_1 t_2 a \cos \phi + (t_1 t_2 a)^2}, \quad (4)$$

where T_d represents the intensity transmission of drop port, a indicates the single-pass amplitude transmission, including both propagation loss in the ring and loss in the couplers and ϕ indicates the single-pass phase shift. With the increase of $t_1 t_2$, the lowest transmission power of drop port $T_{\text{drop,min}}$ and the full width at half maximum (FWHM) decrease, showing a sharper resonance. The relationships are shown in Eqs. (5) and (6).

$$T_{\text{drop,min}} = \frac{(1 - t_1 t_2 a)^2 T_{\text{drop,max}}}{(1 + t_1 t_2 a)^2}, \quad (5)$$

$$FWHM = \frac{(1 - t_1 t_2 a) \lambda_{\text{res}}^2}{\pi n_g L \sqrt{t_1 t_2 a}}, \quad (6)$$

λ_{res} represents the resonate wavelength and L indicates the round trip length. In Fig. 3(c) and Fig. 3(d), three adjusting directions: (i) increasing or (ii) decreasing the coupling coefficient of one side while keeping the other side coupling state unchanged, (iii) decreasing the coupling coefficients of both sides while maintaining $\kappa_1 = \kappa_2$, are shown, realizing flatten peak transmission powers.

Another non-ideal factor is the unsmooth optical spectrum as shown in the inset of Fig. 3(b). These spectral fluctuations arise from unintended light resonating within an extra resonator composed of two half parts of different MRRs and delay lines, which are unavoidable in such cascaded MRRs configuration. When a small weight is needed, the MRR's resonance is tuned away from the processing wavelength. In this case, the high-speed signal is filtered by the slope and unsmooth CMRR-DL transmission spectrum, resulting in additional signal distortion. A viable solution to address this issue is to employ coupling ratio tunable MRR with asymmetric Mach-Zehnder interferometer (AMZI) structure⁴³, as shown in Fig. 3(e). This setup allows for the adjustment of transmission power without shifting the resonator wavelength by tuning the micro heater on AMZI to modify the effective coupling ratio from 0 to $\sim 4\kappa_2(1 - \kappa_2)$. The simulated adjustment process is visualized in Fig. 3(f), where various changes in effective

refractive index Δn_{eff} are applied to the asymmetric waveguide. This approach offers a means to mitigate the additional spectral filtering effect and enhance the system's performance, particularly for applications involving high-speed information transmission or processing.

When employing a parallel multi-wavelength source, the system can perform both high-precision non-negative multiplication and delay-summation operations. For the former operation, the precision of MRR weight control is essential. Several challenges arise due to the cascaded MRRs principle and compact optical and electrical design, including transmission spectra overlap, electrical, and thermal cross-talks. To address these problems, the gradient-descent-based adjustment strategy is used to set weights for each MRR with high precision, as outlined in the flowchart presented in Fig. 3(g). The process involves the following steps. Initially, a set of target weights is specified and the initial voltages are applied according to the pre-established transmission-voltage look-up tables, achieved by sweeping the voltages of each MRR precisely. Due to the cross-talks and other non-ideal factors, the current weights obtained through the optical spectra analyzer (OSA), may not align closely with the ideal weights and the deviations serve as the loss function. Then the GD algorithm is used to acquire the next step voltages, where the gradients are derived from difference calculations. The iterative loop continues until the loss stabilizes or becomes smaller than a predetermined deviation threshold. Figure 3(h) demonstrates the control strategy results for the first 4 MRRs scanning from 0 to 1. Notably, the maximum deviations remain below 1×10^{-3} corresponding to the precision of 9 bits and the details of the calculation method are shown in Supplementary information Section 2. This approach effectively ensures the desired level of precision in multiplication operations.

For the delay-summation operation, multi-wavelength optical carriers are modulated with the same signal and propagate through distinct paths regulated by MRRs, each characterized by a discrete increase in delay time. Then the multi-wavelength optical signals are simultaneously detected by a PD. When the signal rate matches the reciprocal of delay time increment between channels, the signal will be delay-summed as expected. Figure 3(i) presents the active channels to be summed with bright colors and the idle channels in color gray. The idle channels are intentionally shifted away from the operation resonator wavelength to avoid unwanted signal

interactions. The signal rate is set to 8.5 Gbps corresponding to the delay time of two waveguide spirals. **Figure 3(j)** shows the synchronized detected signals from different MRRs paths each with a 1-bit period delay. Signals from the four channels are electrically summed (shown by the black line), and the summed signal closely matches the expected simulated signal depicted in the red line of **Fig. 3(k)**, which demonstrates the effective functionality of the system in accomplishing delay-summation operation.

Application demonstration

This section shows three different applications employed the proposed CMRR-DL signal processing system, working under incoherent/coherent regimes respectively. When this system works as an incoherent architecture, employing the optical frequency comb generated by a nonlinear MRR as parallel multi-wavelength optical source, two applications of tunable microwave photonics (MWP) filter and image edge detection are demonstrated using a similar experimental setup as shown in **Fig. 4(a)**. Either the external-cavity diode laser

(ECDL, Toptica CTL1550) or the InP distributed feedback (DFB) laser with an isolator can be utilized to pump the dark-pulse microcomb as the optical source. The spectrum of the comb line with 2 FSR spacing of 182 GHz pumped by ECDL with proper environment temperature and pump frequency detuning is shown in **Fig. 4(d)**. The initial comb source is amplified by an EDFA and then the desired comb lines are selected using an optical tunable band-pass filter. Light enters and outputs from the silicon chip through vertical grating couplers with an efficiency of about 40%. The silicon chip is packaged onto a custom-designed print circuit board (PCB) as depicted in **Fig. 4(c)** and a thermal-electric cooler (TEC) is utilized to reduce the thermal crosstalk. The output light is split by a 10:90 fiber coupler: 10% of the light is sent to an OSA for monitoring purposes while the other 90% propagates into a photodetector (Finisar HPDV2120R). A low-noise EDFA is used to amplify the off-chip optical signal in MWP filter applications.

For the application of MWP, the TDL-based reconfigurable MWP filters using either non-dispersive (true-time) delay lines or dispersive delay lines are

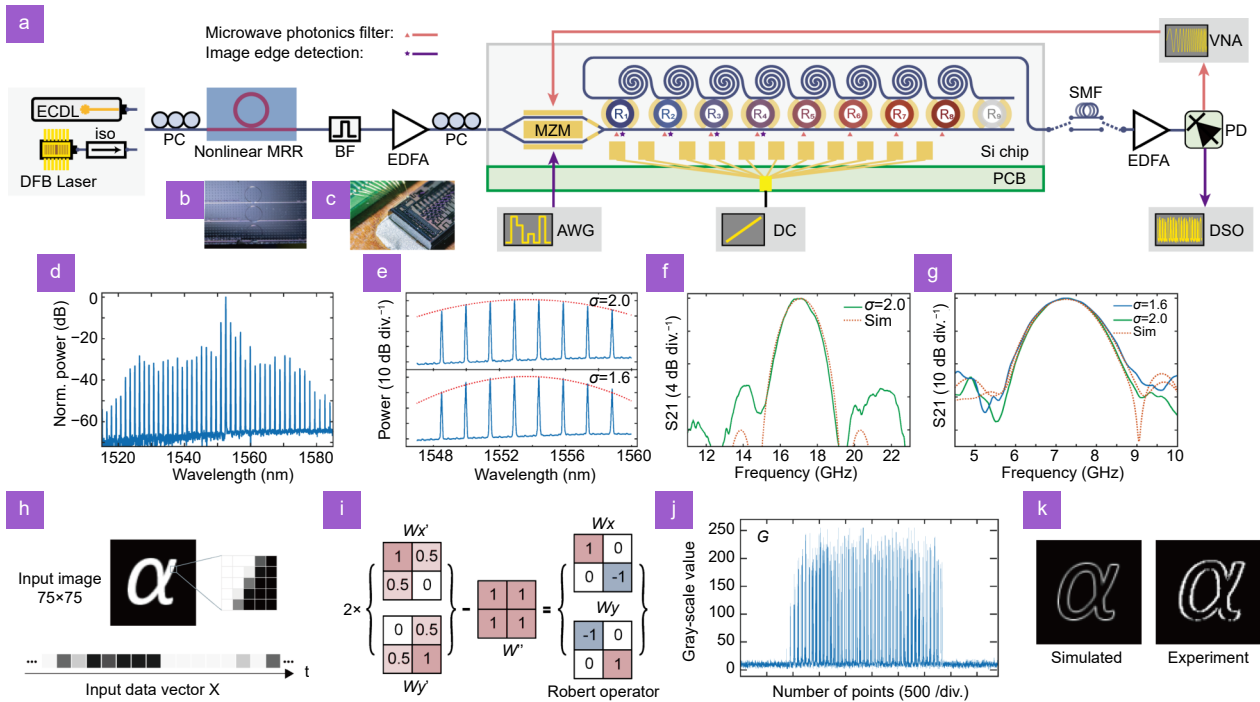


Fig. 4 | Experimental demonstrations of reconfigurable MWP filter and image edge detection. (a–c) Diagram of the experimental setup, lines in red for MWP filter and lines in purple for image process. Optical images of (b) Nonlinear MRR and (c) packaged SOI chip. (d) Optical spectrum of optical frequency comb used as parallel multi-wavelength source generated by nonlinear MRR. (e–g) Reconfigurable MWP filter results. (e) Optical spectra of comb lines with Gaussian envelope, adjusted by the CMRR-DL system. RF filtering response (f) in the non-dispersive delay scheme and (g) in the dispersive delay scheme. (h–k) Image edge detection results. (h) The picture of symbol alpha used as the input image. (i) Two 2x2 kernels (Roberts operator) for edge detection. (j) Measured time-series data. (k) Detected image edge from simulation and experiment.

demonstrated. The vector network analyzer (VNA, Keysight N5247A) is employed to characterize the RF responses. Eight comb lines are utilized as taps and modulated by the on-chip MZM with a 9-dBm frequency-swept RF signal from VNA. By tuning the optical spectra with a Gaussian envelope as depicted in Fig. 4(e), the expected RF filtering responses can be detected by the PD. Results in Fig. 4(f) show the experimental and simulated RF responses in the non-dispersive delay scheme, where the Gaussian parameter σ is set to 2. The 3-dB passband bandwidth (BW) is 2.04 GHz and the main-to-sidelobe suppression ratio (MSSR) is more than 10 dB. In the dispersive delay scheme, on-chip waveguide delay lines are replaced by a spool of 5-km single-mode fiber to accumulate dispersive delay between comb lines. With the Gaussian parameter of comb lines optical spectra changing from 2.0 to 1.6 as shown in Fig. 4(e), the RF 3-dB passband BW can be adjusted within the range of 1.08–1.14 GHz, while maintaining the MSSR over 20 dB, presented in Fig. 4(g).

In the application of image edge detection, the image convolution operation is used with the Roberts operator, consisting of two 2×2 convolution kernels. This operation can be viewed as a form of matrix multiplication. By sliding the two kernels over the image, two output images (G_x and G_y) are generated highlighting edges of $+45^\circ$ -direction and -45° -direction respectively. The gradient magnitude at each pixel is calculated by the formula: $G = \sqrt{G_x^2 + G_y^2}$. For this operation, four comb lines are selected corresponding to the kernel matrix size $n = 4$. To apply this operation using the silicon chip, the input image, in this case, the image of the Greek alphabet ‘ α ’ is firstly converted into a 70×70 gray pixel matrix and normalized to fall within the range $[0, 1]$. The pixels in the sliding window are serialized to form an input image vector aligning with the sliding path of kernels. Subsequently, the input image vector is converted into analog electrical signal using an arbitrary waveform generator (AWG, Tektronix AWG70001) and then amplified by a pair of linear electrical drivers (SHF 807C). The signal is further encoded into the intensity of the 4 used comb lines simultaneously by the silicon EOM. The signal rate is set to be 17 Gaud, meeting the waveguide’s delay time. Because the information regarding the kernel weights is encoded into the transmission ratio of the MRRs, only positive weights can be utilized in this process. To realize computation in the complete real-number domain, the original convolution computing can be

substituted with two steps as shown in Fig. 4(i). After the four comb lines with serialized image information propagating the CMRR-DL system with kernel weights loaded by the MRRs, the intensity of output lights carries the convolution results. The resulting RF signals from PD are received by a real-time oscilloscope (RTO, Keysight DSA-X 96204Q). The measured time-series data containing the image edge information is shown in Fig. 4(j). After conducting serial-to-parallel conversion and subtraction operations on a computer, the edge detection result is presented in Fig. 4(k), which agrees well with the ideal result, confirming the system’s ability to perform convolution processes effectively.

The programmable on-chip silicon processor can also work as a low-cost optical equalizer. Currently, the signal processing capability in the electrical domain is limited by the microelectronic ADC processor⁴⁴, which is also restricted by the advanced lithography technology. Comparing with the expensive signal processing in the electrical domain, optical spectral shaping can be realized with optical filters²⁰. As a core component for the integrated transceiver, silicon modulators’ performance plays a key role in optical telecommunication and interconnect systems. The modulators’ design still struggles with the tradeoff between modulation efficiency and response speed. Moreover, modulators’ efficiency is also restricted by the capability of CMOS-compatible driver especially when operating at a higher data rate⁴⁵. Due to the limited electro-optical response speed, the expansion of data capacity has stepped into a slow development era.

With the flexible processor architecture, quasi-arbitrary optical spectral shaping can be realized by the CMRR-DL system. The experimental setup is shown in Fig. 5(a). By tuning the optical response around the carrier wavelength, as shown in Fig. 5(b), the proposed on-chip processor could work in the mode that reshapes the modulated signal in the frequency domain, which is essentially the reason to enhance the bandwidth-limited devices. The measured S21 response curve for the silicon MZM with and without the on-chip equalizer is depicted in Fig. 5(c). The 3-dB bandwidth improves from 27 GHz to nearly 60 GHz. Additionally, to further display the improvement of the bandwidth-limited silicon modulator, eye diagrams of on-off-keying (OOK) modulation format at 66 Gbps are demonstrated in Fig. 5(d, e). The Q-factor, as a measure of the eye-opening⁴⁶, is also improved from 1.88 to 2.90, highlighting the effectiveness of the on-chip equalizer in enhancing signal quality.

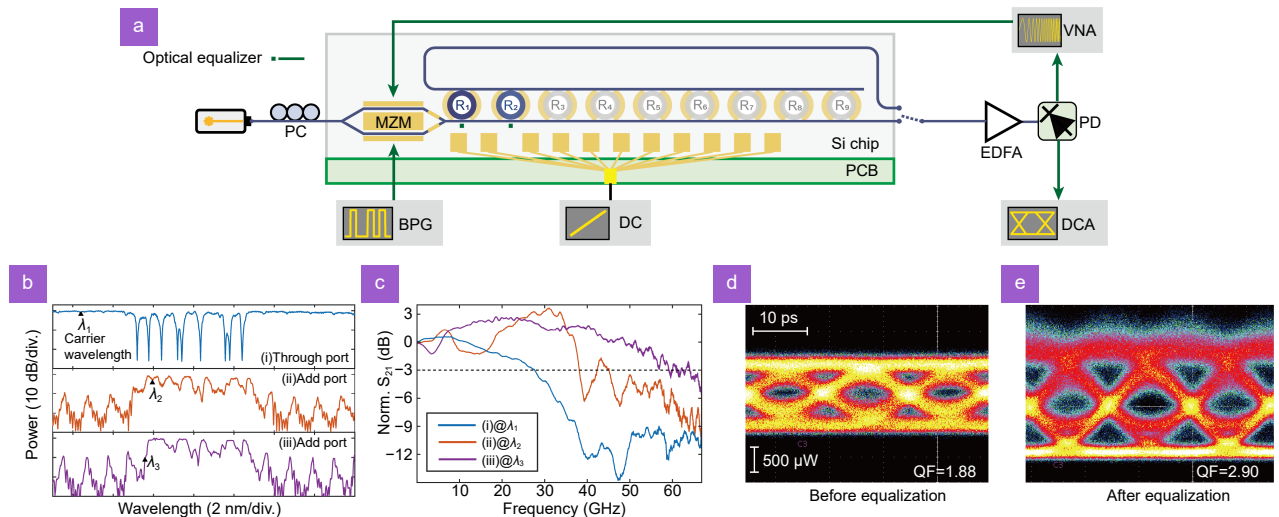


Fig. 5 | Experimental demonstrations of the low-cost optical equalizer. (a) Diagram of the experimental setup. (b) Optical spectra of the CM-RR-DL system and optical carrier frequency under different conditions: (i) at the flat region of the through port, (ii) in the center of two rings' resonances of the drop port, (iii) at the slope region of the drop port. (c) Normalized S_{21} under different conditions. (d, e) Eye diagrams and Q-factors (d) before and (e) after equalization.

Discussion

In this paper, we present a multi-functional and highly reconfigurable monolithic processor fabricated on the SOI platform and conduct in-depth analyses of the system. The processor leverages a silicon MZM in conjunction with the CMRR-DL processing core. Such system imparts tunability and versatility and works in a mode having both the excellent specialized performance characteristic of the ASPIC architecture and the flexible reconfigurability of the FPPGA architecture. The processing core provides tunable optical filtering and optical true time delay, supporting both coherent analog and incoherent digital processing, which is applicable to different scenarios. The utilization of multi-wavelength source enables the realization of high-speed universal matrix multiplication, encompassing steps of elements multiplication and summation, and the precision of multiplier loaded by MRRs can reach up to 9 bits. In this case, we explore the versatile functionalities of the processing system in applications of reconfigurable MWP filter with tunable 3-dB BW and photonic matrix computing for image edge detection with an impressive speed of 17 GHz. Additionally, for single-wavelength carriers, the processor behaves as a low-cost optical equalizer, realizing 3-dB EO bandwidth and eye diagram improvement of silicon MZM. This monolithic processor showcases the convergence of high performance, configurability, and versatility, offering a promising solution for diverse on-chip information processing applications.

The performance of the monolithic silicon photonic system can be further enhanced by employing superior architecture design and optimized photonic devices. First, to achieve a higher MWP filter suppression ratio, accommodate larger matrix size, and reduce cross-talks, it's essential to widen the FSR of MRRs for more wavelength channels and larger channel space. Several structures have been reported to realize FSR-free MRRs, such as grating-assisted contra-directional couplers⁴⁷, MZI-coupled⁴⁸ and reflector-embedded⁴⁹ microrings. Second, the processing speed of the current system is fundamentally constrained by the modulation and detection rates. Therefore, large bandwidth modulator^{50,51} and high-speed PD^{52–54} based on SOI are needed and the recently reported works have promised a potentially higher processing speed of the system. In the meantime, due to a higher data rate, the waveguide delay time will be shorter, which will achieve a smaller footprint and improve the degree of integration. Third, to minimize the distortions of high speed signal caused by the relatively narrow linewidth of conventional MRRs, cascaded MRRs⁵⁵ and MZI-embedded⁴³ structure can be utilized for flat-top pass band and tunable coupling ratio, supporting high-speed data loading and weight tuning. Fourth, more functions and applications based on the system can be exploited. Typical signal processing functions such as first-order differentiation, integration, and Hilbert transform, can be realized based on the TDL architecture^{56–58}. Another potential functional upgrade is to implement

on-chip balanced PD connecting to the drop ports of two CMRR-DL systems for operations in the real number domain, which can double the computing speed compared to the current architecture. Besides, working at single-wavelength conditions, the TDL structure can be regarded as a transversal filter which is commonly used for eliminating ISI in optical fiber communication, as mentioned in Section *System architecture and principle*. These optimizations and expansions on both device-level and system-level as well as extended application scenarios would further change the design method and improve the application value of integrated photonic chips.

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Author contributions

The experiments were conceived by YC Wu. The simulation and analyses were conducted by YC Wu. The characterizations of devices and systems are performed by YC Wu, with assistance from QP Yang, YS Tao, BT Shen and XG Zhang. The optical computing experiment was performed by YC Wu, QP Yang, BW Bai and HW Shu, with assistance from BT Shen. The optical communication equalization experiment was performed by YC Wu, TT Li and HW Shu, with assistance from LW Xing. The microwave photonics experiment was performed by HW Shu and YS Tao, with assistance from BT Shen and ZH Tao. The microcomb generation is performed by HW Shu and BT Shen. The devices were designed by HW Shu and YS Tao. The electrical packaging was accomplished by ZF Ge and ZH Tao. The results were analysed by YC Wu, QP Yang, BT Shen, YS Tao, XG Zhang, ZH Tao, TT Li, BW Bai and HW Shu. All authors participated in writing the manuscript. The project was under the supervision of TT Li, BW Bai, HW Shu and XJ Wang.

Competing interests

The authors declare no competing financial interests.

Supplementary information

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