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Integrated optical transceivers: from advances to deployment

Changhao Han¹ and Linjie Zhou^{2*}

Abstract: The rapid growth of artificial intelligence and high-performance computing is imposing increasingly stringent demands on the bandwidth density, latency, and energy efficiency of data movement. In a recent review, Peng Yan and colleagues provide a systematic overview of integrated optical transceivers, covering their architectural evolution, key transmitter and receiver technologies, integration approaches, and emerging applications. By relating device and circuit technologies to transceiver architectures and target applications, the review offers an integrated perspective on optical interfaces spanning pluggable modules, co-packaged optics, and optical input/output. Future progress will increasingly rely on cross-layer co-design, scalable manufacturing, thermal management, testing, and interface standardization.

Keywords: integrated optical transceiver; silicon photonics; optical interconnects; co-packaged optics; optical input/output

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The rapid expansion of artificial intelligence (AI) and high-performance computing (HPC) is changing both the scale and organization of modern computing infrastructure¹. Scale-out systems connect increasing numbers of servers, switches, and accelerator nodes, while scale-up systems require dense links among processors, accelerators, and memory resources. These developments are driving rapid traffic growth across an interconnect hierarchy extending from data-center networks and fabrics to boards, packages, and chips. As lane rates increase, copper-based electrical links face greater channel loss, crosstalk, and signal-integrity degradation. Complex equalization and retiming can extend their operating range, but they also increase power consumption and system complexity². By contrast, optical links offer higher bandwidth density and lower propagation loss, with reduced reliance on power-hungry electrical equalization as reach increases. Optical interconnects are therefore moving progressively closer to computing and switching chips³. In this context, Peng Yan and his colleagues present a timely review that examines integrated optical transceivers from the perspectives of architectures, enabling technologies, and target applications⁴.

At the architectural level, the review traces the integra-

tion-driven evolution of optical transceivers. Conventional pluggable modules have enabled large-scale deployment of optical links through standardized form factors, interoperability, and field replaceability. However, as switch and accelerator bandwidths continue to rise, the electrical paths between host chips and front-panel modules impose increasing penalties in power consumption and signal integrity while limiting bandwidth density. Linear drive pluggable optics (LPO) modules reduce or eliminate module-level digital signal processing overhead. Near-packaged optics (NPO) place optical engines close to the host package, shortening high-speed electrical paths. Co-packaged optics (CPO) further integrate optical engines adjacent to the host chip within the same package, enabling tighter electrical-optical integration⁵. The interconnect hierarchy and representative transceiver integration schemes are illustrated in Fig. 1. Optical input/output (OIO) brings optical connectivity to the package or chiplet level, allowing optical engines to be integrated more closely with processors and accelerators⁶. Importantly, these architectures address different combinations of reach, bandwidth density, power consumption, serviceability, and cost. They should therefore be viewed as complementary solutions for different system requirements

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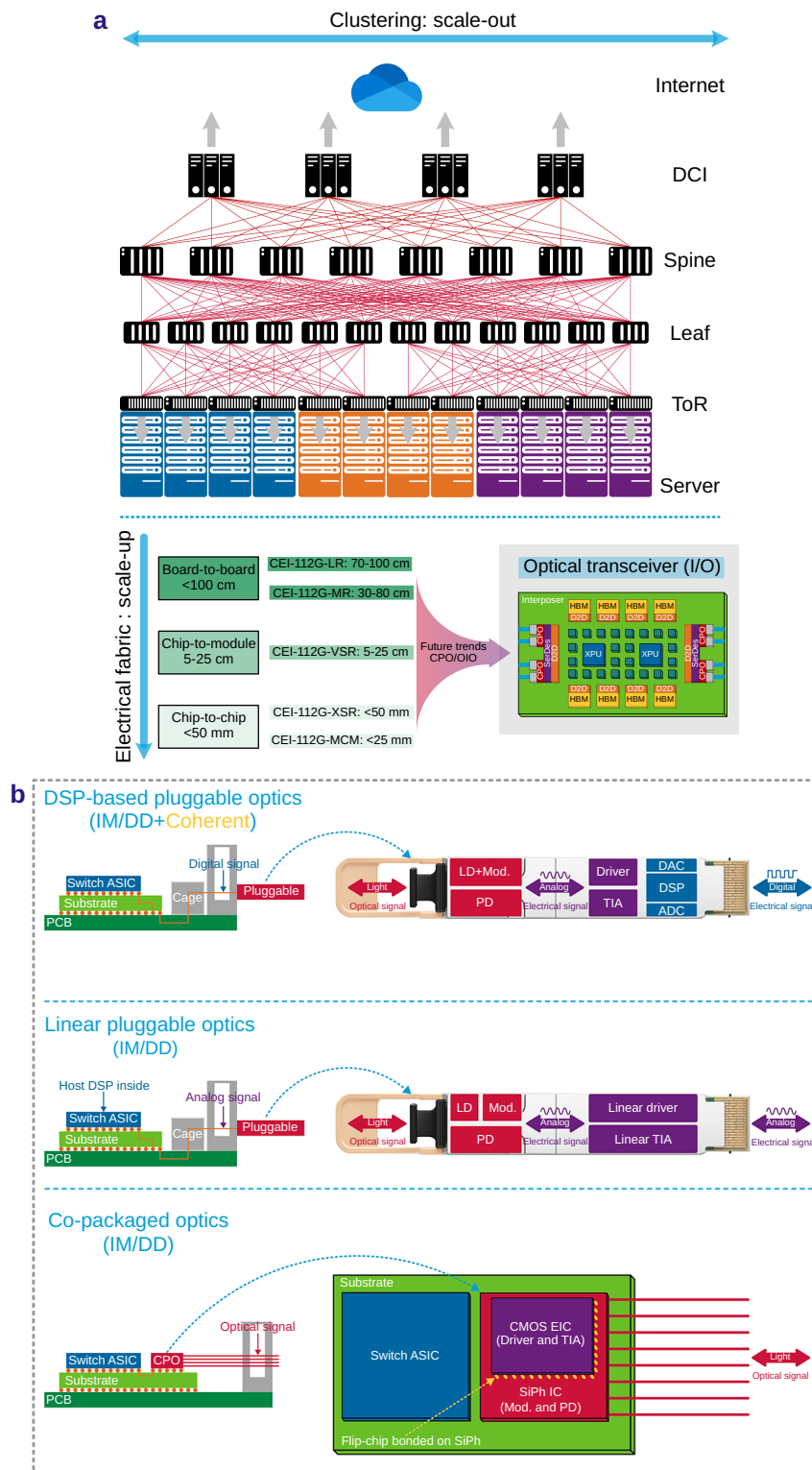


Fig. 1 | Optical interconnect hierarchy and representative transceiver integration schemes for modern computing systems. (a) Scale-out network hierarchy from servers and top-of-rack switches through leaf and spine layers to data-center interconnects, together with scale-up links spanning board-to-board, chip-to-module, and chip-to-chip reaches. (b) Representative architectures for DSP-based pluggable optics, linear pluggable optics, and co-packaged optics, which differ in the partitioning and physical placement of digital processing, data conversion, analog front-end, and photonic functions. In linear pluggable optics, digital signal processing is moved to the host while the module retains a linear electrical interface, whereas co-packaged optics places the optical engine close to the switch ASIC within a common package, thereby shortening high-speed electrical interconnects. Figure reproduced from ref. ⁴, under a Creative Commons Attribution 4.0 License.

rather than a simple replacement sequence.

At the technology level, the review surveys the key photonic devices and electronic circuits that form integrated transmitters and receivers. On the transmitter side, it discusses solutions based on directly modulated vertical-cavity surface-emitting lasers (VCSELs), electro-absorption modulated lasers (EMLs), Mach-Zehnder modulators (MZMs), and microring modulators (MRMs), together with their associated complementary metal-oxide-semiconductor (CMOS) and silicon-germanium (SiGe) driver circuits. These transmitter technologies present different trade-offs in bandwidth, drive requirements, linearity, thermal sensitivity, and integration compatibility. For example, a study of a single-drive push-pull silicon MZM illustrated how device structure and drive configuration influence modulation linearity and multilevel pulse-amplitude modulation performance⁷. On the receiver side, the review covers single-ended and balanced photodetectors (PDs), transimpedance amplifiers (TIAs), and receiver architectures for both intensity-modulation/direct-detection (IM/DD) and coherent links. PD responsivity and capacitance must be considered together with the noise, bandwidth, and linearity of the TIA. Co-design of PDs and electronic front ends can reduce interface parasitics and improve overall energy efficiency⁸. These examples illustrate the importance of evaluating photonic devices and electronic circuits within the complete transceiver signal path.

Importantly, the review also relates these technologies to their target applications. Integrated optical transceivers already play an important role in data-center and HPC fabrics, including links involving accelerators and high-bandwidth memory. Integrated photonic platforms are also extending optical connectivity beyond conventional fibre links toward fibre-wireless convergence, enabling high-capacity transmission across both wired and wireless domains⁹. Beyond these core application areas, the review discusses their potential use in short-reach free-space links, Internet of Things and edge systems, autonomous vehicles, and quantum communication. By considering transceiver architectures and enabling technologies in the context of these applications, the review provides a broad view of the expanding roles of integrated optical transceivers across computing, sensing, and communication systems. Its value lies not only in summarizing advances in transceiver architectures, devices, and circuits, but also in relating these advances to diverse application requirements.

Future integrated optical transceivers will require progress at several interconnected levels. CPO, OIO, and chiplet-based optical engines offer promising routes toward higher bandwidth density and lower electrical I/O energy per bit. Advanced bonding and three-dimensional integration can reduce interconnect parasitics between electronic and photonic dies¹⁰, but tighter integration also introduces challenges in thermal management, power delivery, manu-

facturing yield, optical coupling, and testability. Standardized chiplet interfaces and scalable methods for known-good-die testing will be important for translating laboratory demonstrations into deployable platforms. Roadmaps for Si photonics similarly emphasize that device advances must be accompanied by progress in electronics, packaging, and manufacturing¹¹. Integrated optical transceivers are thus evolving from collections of separately optimized devices toward integrated optoelectronic engines designed at the system level. As these engines move closer to processors and accelerators, optical interfaces will increasingly become system-defined, with their performance jointly shaped by photonic devices, electronic circuits, packaging, system architecture, and application requirements.

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