集成光子卷积加速核助力可穿戴设备革命

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可穿戴设备以其便携性和强大的人机交互能力为特点，长期以来一直代表着技术和创新的未来。光学神经网络 (ONNs) 研究已成为解决电子计算瓶颈的潜在突破性解决方案。微环谐振器 (MRR) 的阵列方法展现了在可穿戴设备领域应用的较大潜力。

华中科技大学国家光电研究中心由董建绩教授带领的课题组提出了一种基于自校准功能的可重构 MRR 阵列的可扩展的光学卷积加速核 (PCAC)。该系统通过对于多波长光信号的复用与 MRR 上的权重矩阵完成乘法运算，在课题组开发的自校准 MRR 阵列的作用下，通过使用平衡光电探测器 (BPD) 进行加权求和而得到最终计算结果，并将光功率差值重建输出得到卷积结果。制造了 4×4 MRR 阵列的概念验证 PCAC 芯片，并成功使用芯片进行了图像边缘提取测试，以及 AR 和 VR 设备等典型可穿戴应用中的光电计算实验：基于深度信息的第一人称视角手势识别。通过用并行光电卷积计算取代电子计算，该工作实现了高效、高精度的计算。

该系统能以光速进行高精度计算，在保持极低功耗的同时实现 7 位精度。在并行处理中，它的峰值吞吐量也达到了 3.2 TOPS (每秒 tera 运算)。

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Integrated photonic convolutional acceleration core revolutionize wearable devices

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Wearable devices, characterized by their portability and powerful human-computer interaction, have long represented the future of technology and innovation. Optical neural networks (ONNs) research has emerged as a potential breakthrough solution to address the bottleneck of electronic computing. The array approach using micro-ring resonator (MRR) devices shows greater potential for application in the field of wearable devices.

The research group of Prof. Jianji Dong at the Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology (HUST) has made progress in integrated photonic convolution acceleration chips based on micro-ring arrays. This work presents a scalable optical convolution acceleration core (PCAC) based on reconfigurable MRR arrays with self-calibration capabilities. The system accomplishes the multiplication operation by multiplexing the multiwavelength optical signals with the weight matrix on the MRR, and the final computational results are obtained by weighted summation using balanced photodetectors (BPDs) under the self-calibrating MRR arrays we have developed, and the convolutional results are obtained by reconstructing the output of the optical power difference.

The system is capable of performing high-precision calculations at the speed of light, achieving 7-bit accuracy while maintaining extremely low power consumption. It also achieves a peak throughput of 3.2 TOPS (tera operations per second) in parallel processing.

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